

8

7

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1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, MBP 15 " MLB

12/07/2007

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N/A

N/A

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BOM Configuration

N/A

N/A

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N/A

N/A

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ENG APPD

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SCHEM / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7413	1	SCHEM,TAUPO,M87	SCH	CRITICAL	
820-2249	1	PCBF,TAUPO,M87	PCB	CRITICAL	

DRAWING

TITLE=MLB

ABBREV=DRAWING

LAST_MODIFIED=Wed Dec 12 10:44:22 2007

DIMENSIONS ARE IN MILLIMETERS

XX : _____

X.XX : _____

X.XXX : _____

ANGLES : _____

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER	/	DESIGN CK	/
ENG APPD	/	MFG APPD	/
QA APPD	/	DESIGNER	/
RELEASE	/	SCALE	NONE
MATERIAL/FINISH		SIZE	D
NOTED AS		APPLICABLE	

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TITLE

SCHEM,TAUPO,M87

DRAWING NUMBER

051-7413

REV

16.0.0

SHT

1

OF

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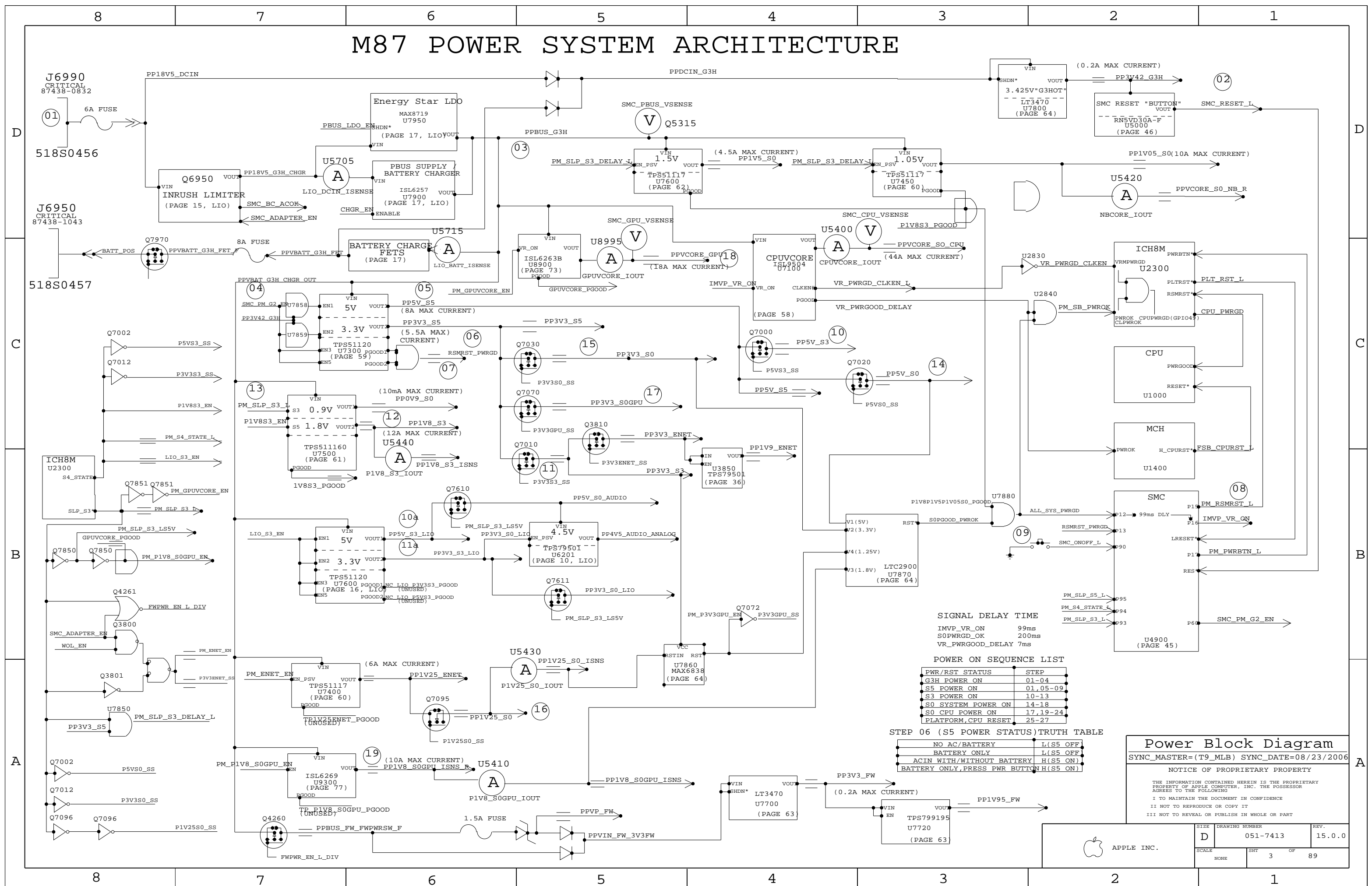
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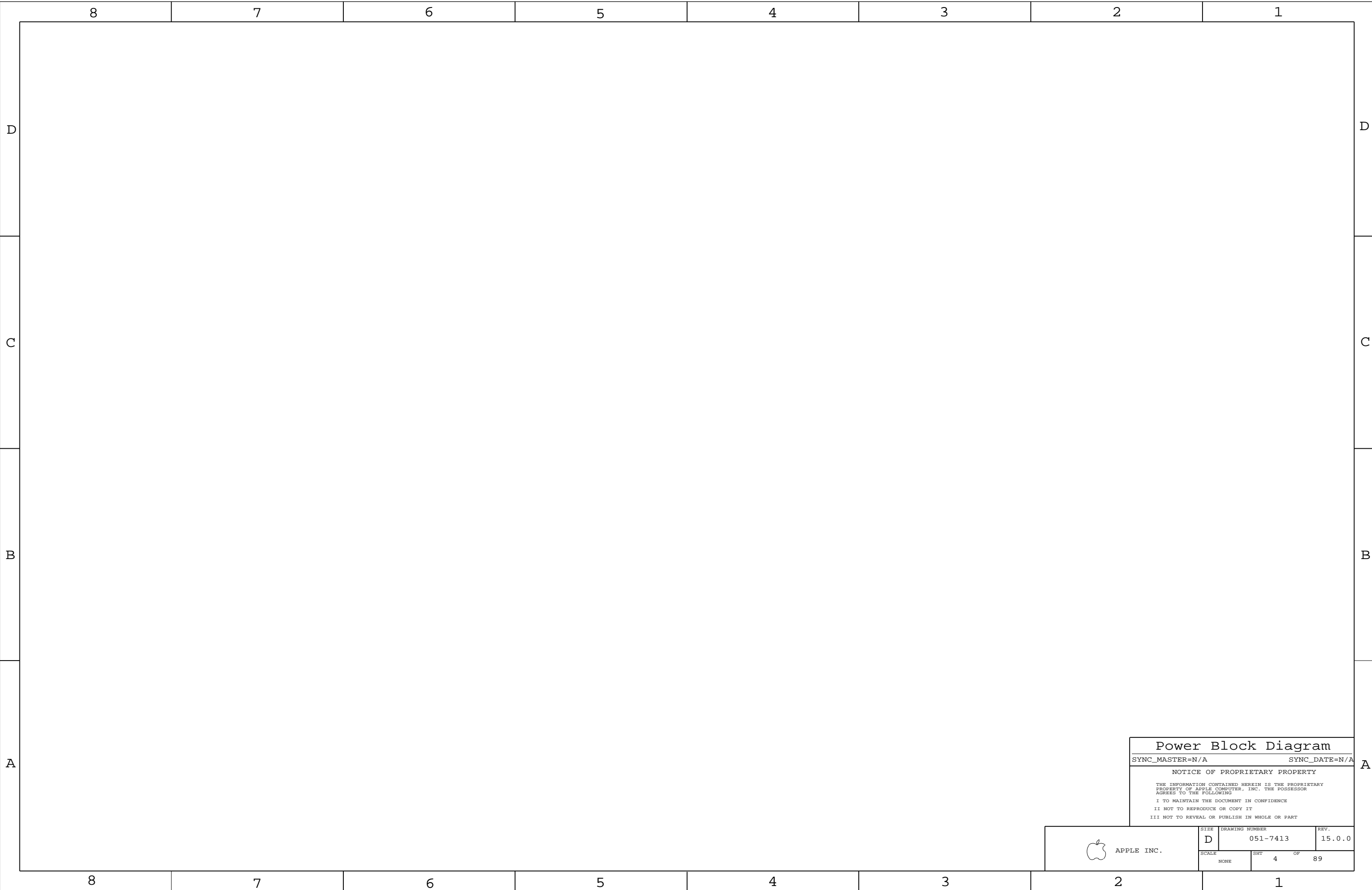
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M87 POWER SYSTEM ARCHITECTURE

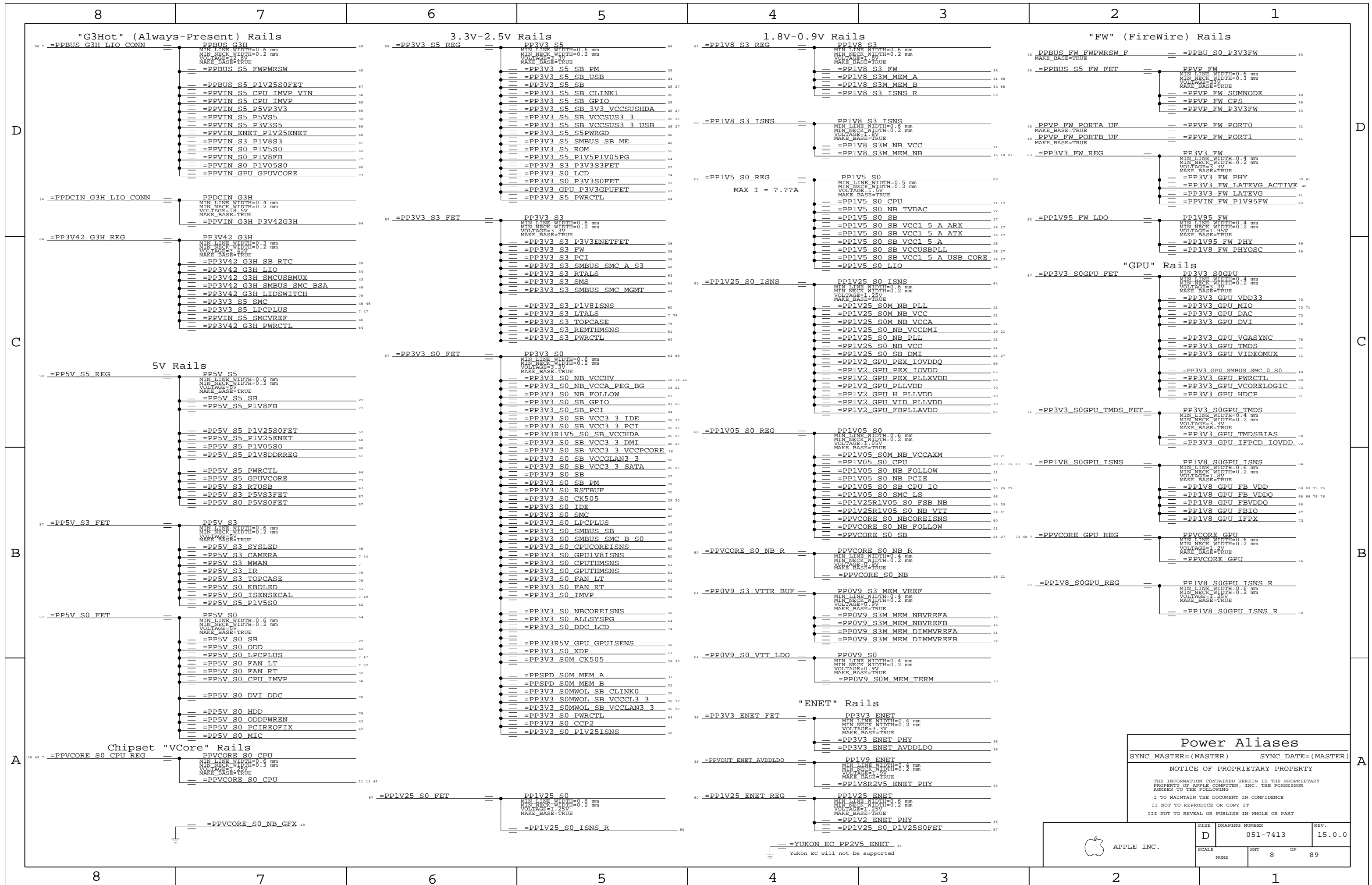


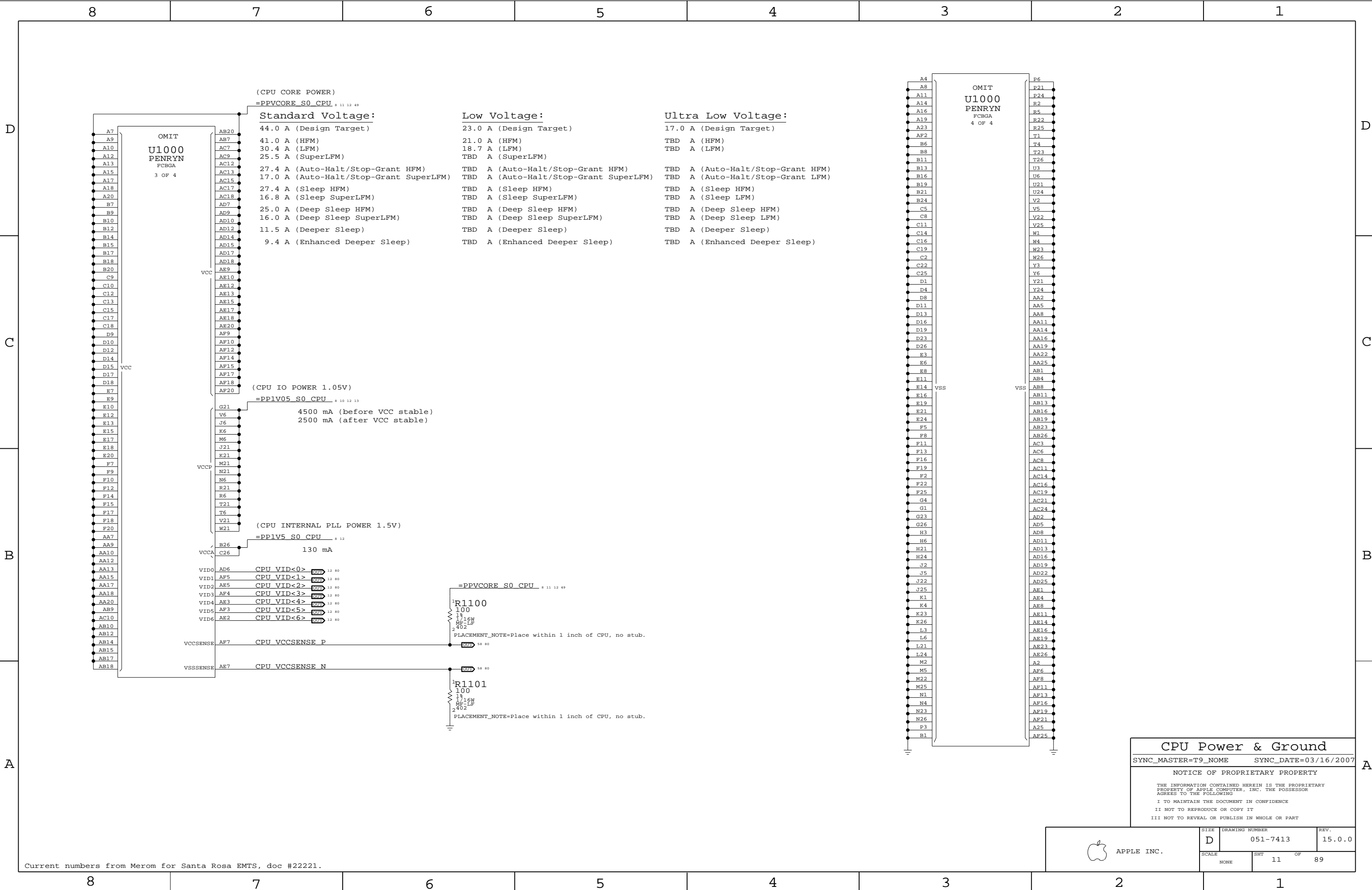


 APPLE INC.	SIZE D	DRAWING NUMBER 051-7413	REV. 15.0.0
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Power Block Diagram		
SYNC_MASTER=N/A SYNC_DATE=N/A		
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[illegible]





D

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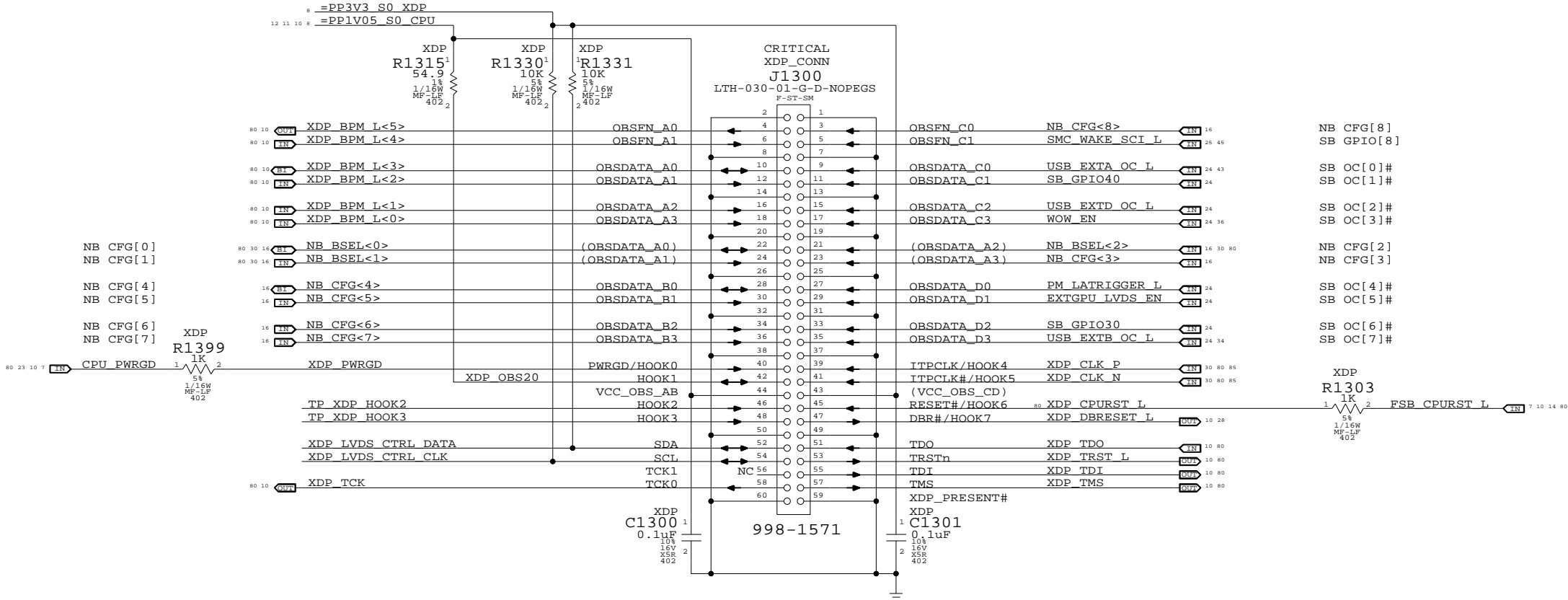
C

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A

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_NOME SYNC_DATE=12/12/2006

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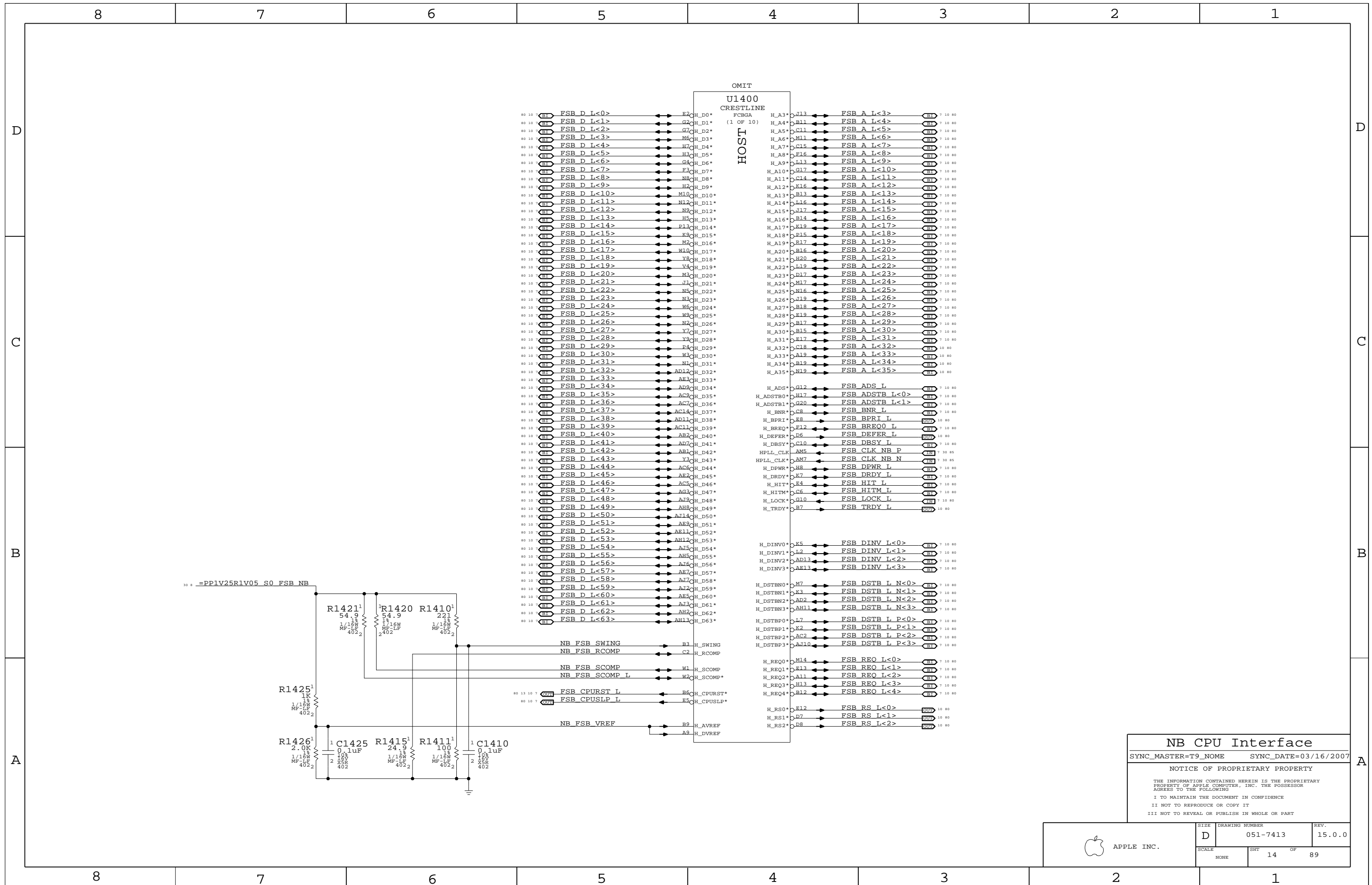
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SCALE	SHT	OF
NONE	13	89



D

C

B

A

D

C

B

A

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

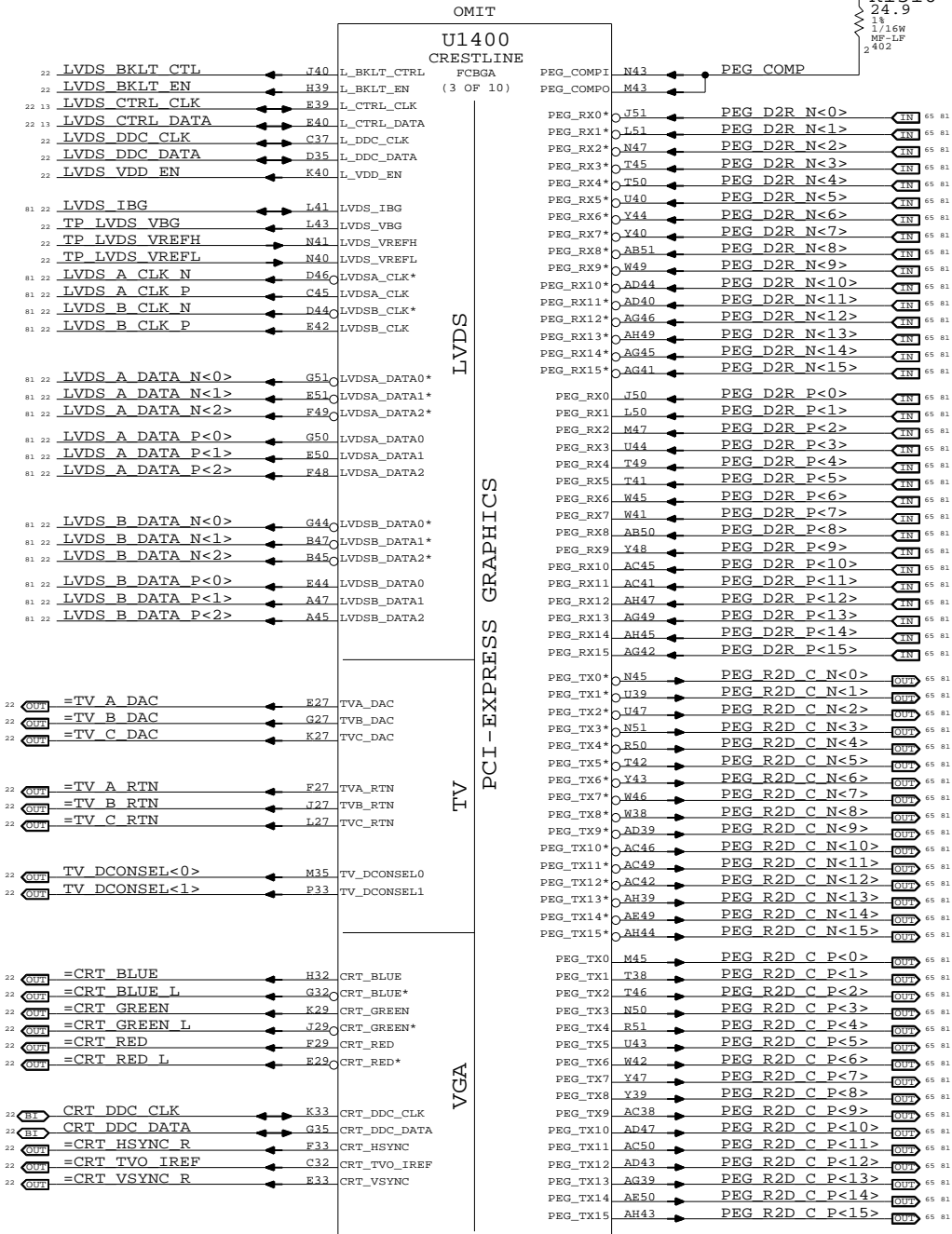
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

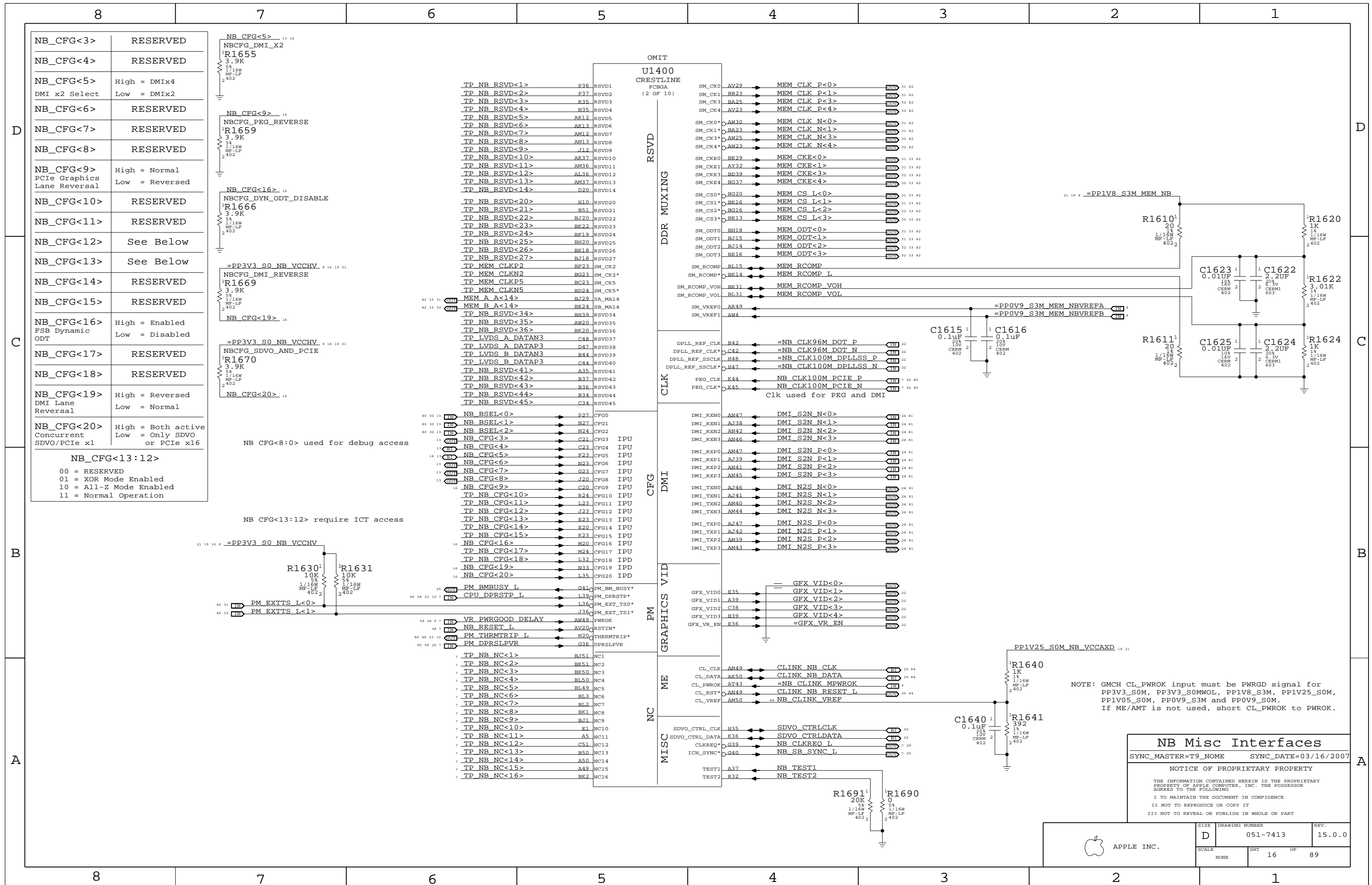
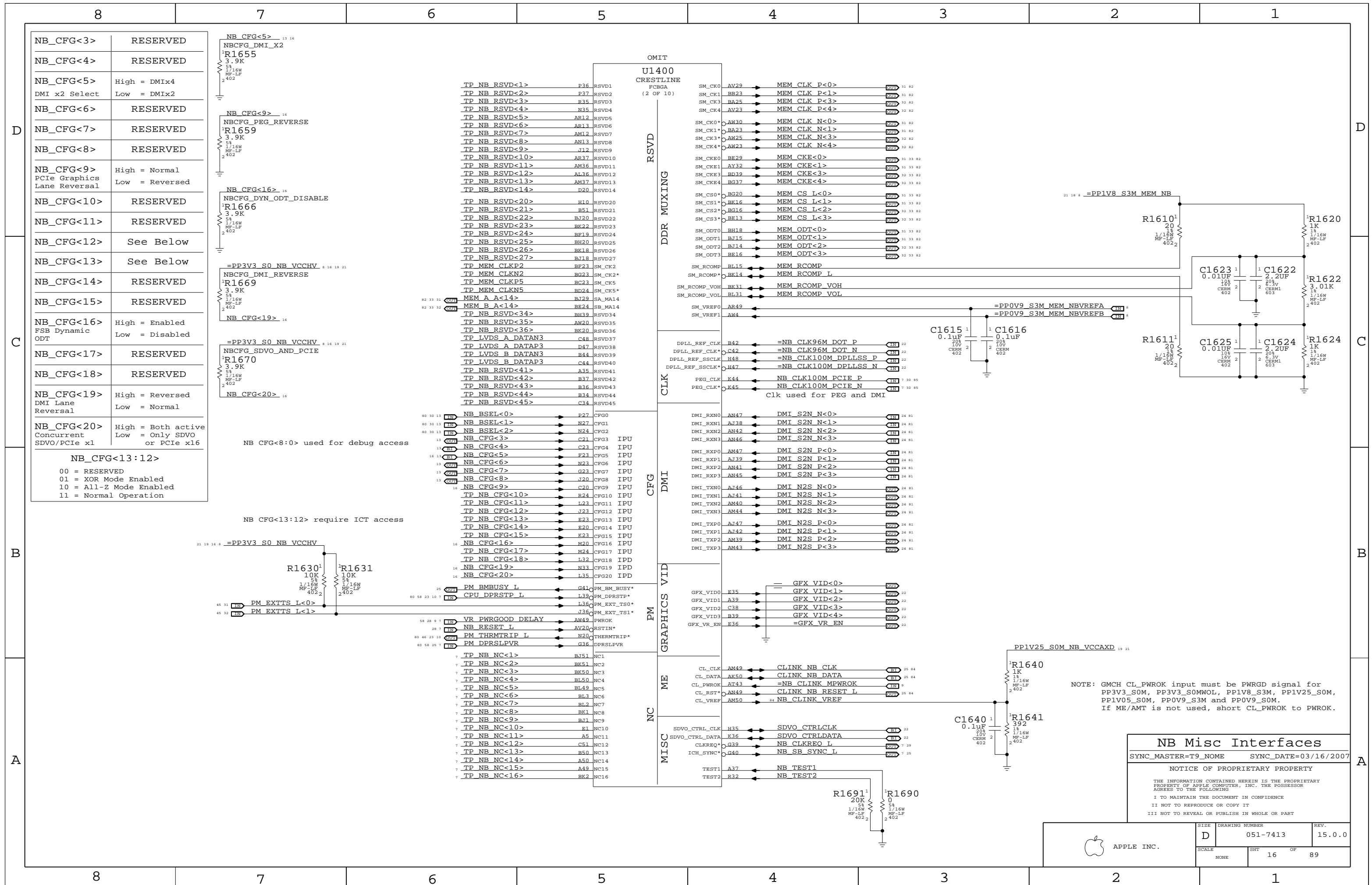
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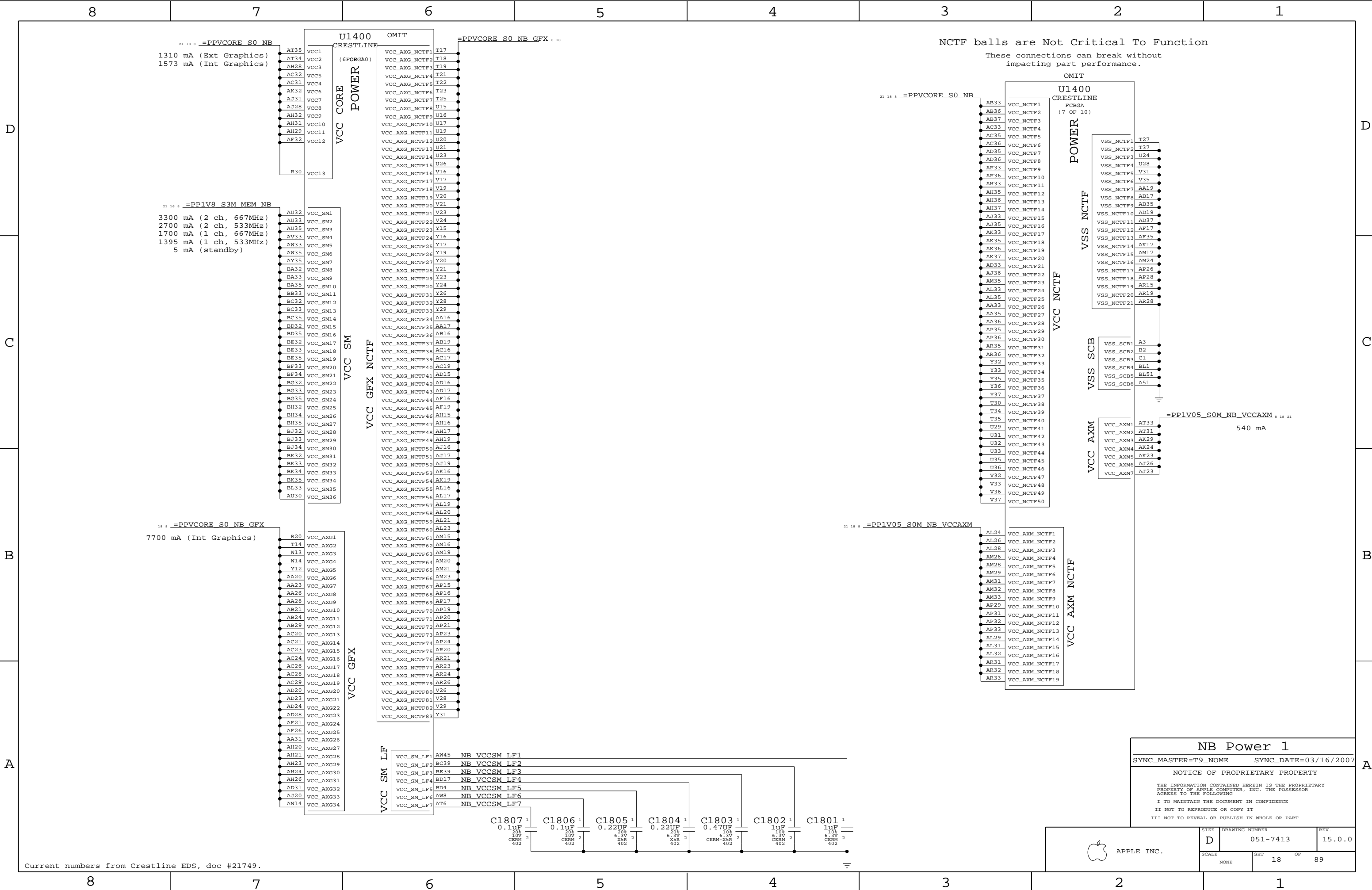


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NONE	15	89



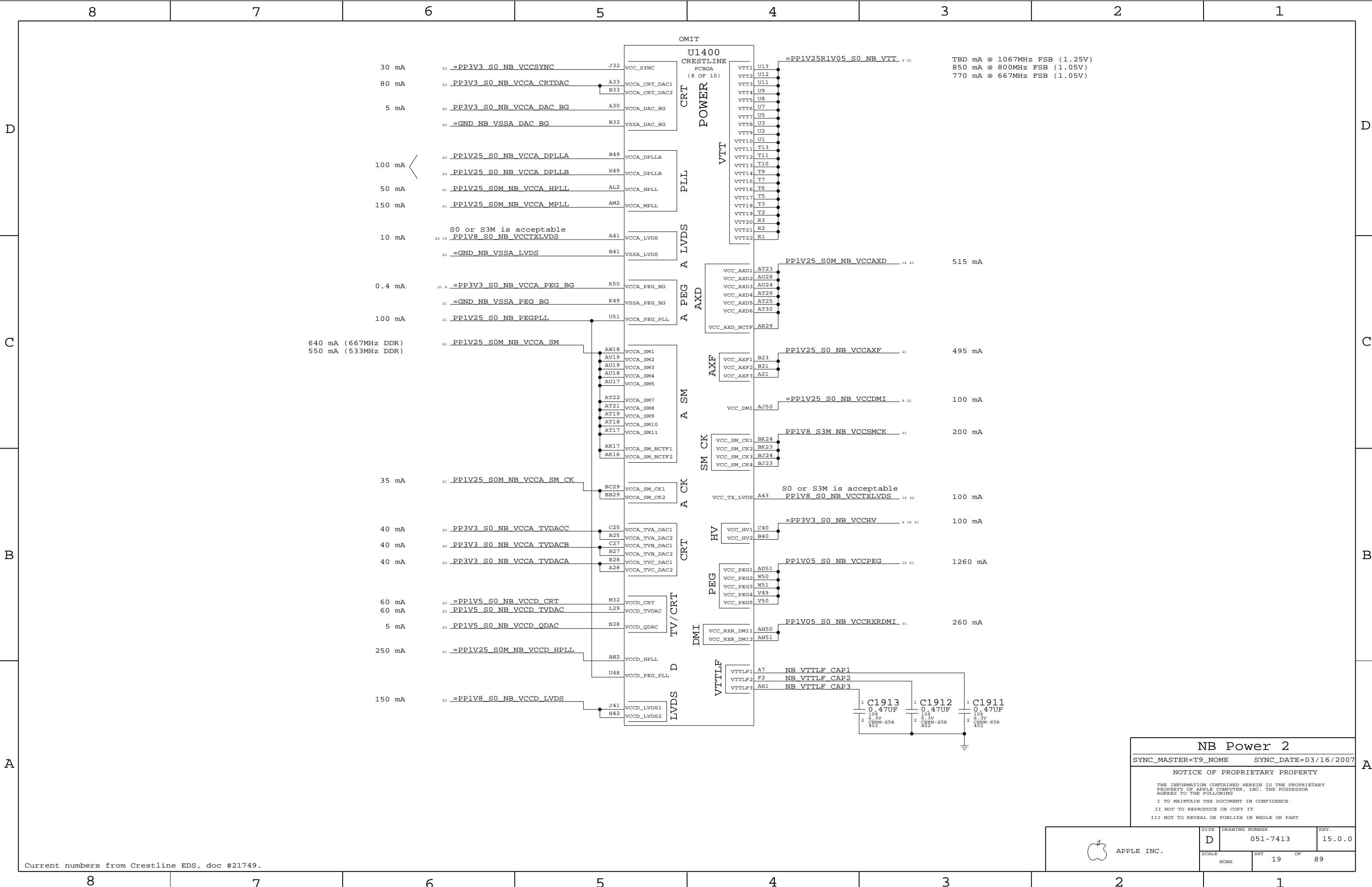




Current numbers from Crestline EDS, doc #21749.

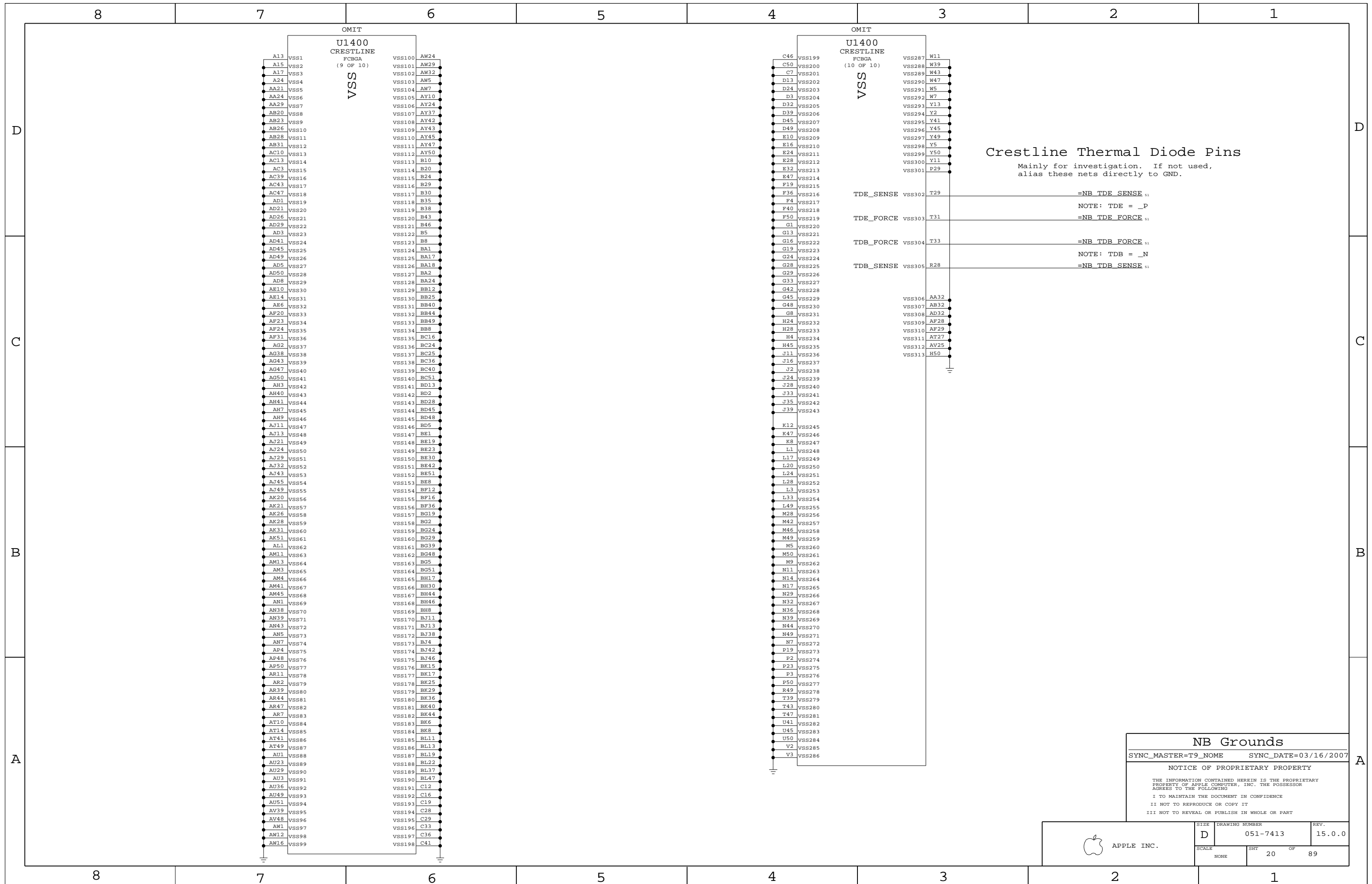
NB Power 1		
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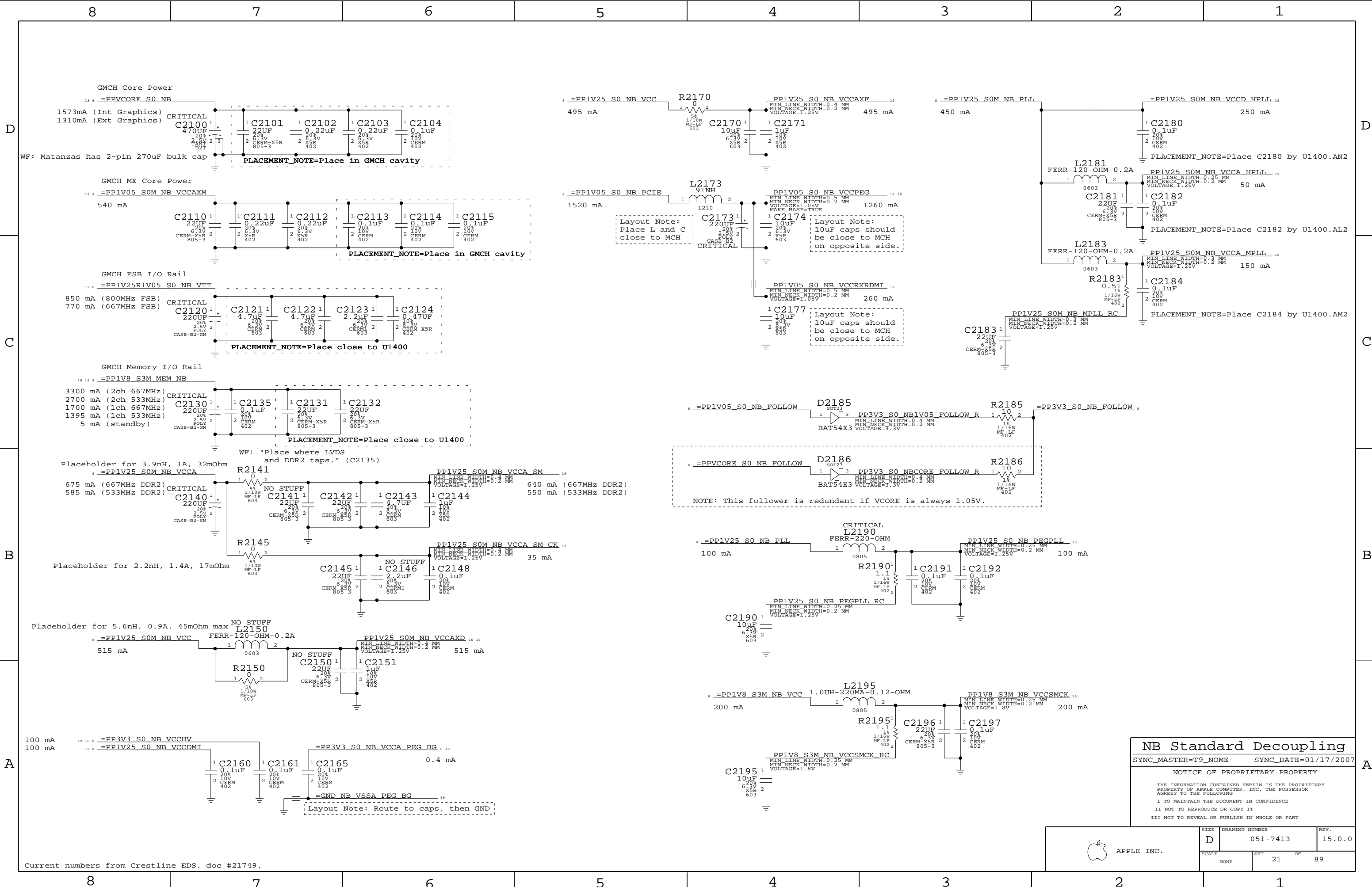
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NB Power 2
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NB Standard Decoupling

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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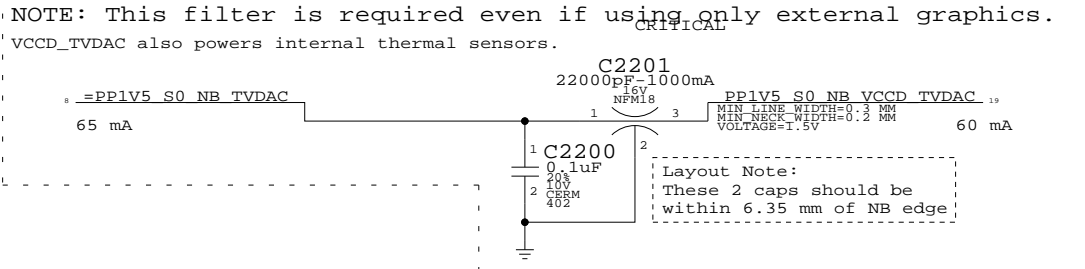
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SCALE	SHT	OF
NONE	21	89

Crestline LVDS Strapping



Layout Note:
These 2 caps should be
within 6.35 mm of NB edge

```

15 LVDS DDC CLK
15 LVDS DDC DATA
15 LVDS CTRL CLK
15 LVDS CTRL DATA
15 =CRT RED
15 =CRT RED L
15 =CRT GREEN
15 =CRT GREEN L
15 =CRT BLUE
15 =CRT BLUE L
15 =CRT HSYNC R
15 =CRT VSYNC R
15 =CRT TVO IREF
15 =TV A DAC
15 =TV A RTN
15 =TV B DAC
15 =TV B RTN
15 =TV C DAC
15 =TV C RTN
15 CRT DDC CLK
15 CRT DDC DATA
15 SDVO CTRLCLK
15 SDVO CTRLDATA
15 TV DCONSEL<0>
15 TV DCONSEL<1>
15 =NB CLK96M DOT N
15 =NB CLK96M DOT P
15 =NB CLK100M DPFLSS P
15 =NB CLK100M DPLLSS N

```

```

--GND NB VSSA LVDS                                     14
--P11V8_S0_NB_VCTCTLVDS                                 14
--P11V25_S0_NB_VCCA_DPLLB                                14
--P11V25_S0_NB_VCCA_DPLLA                                14
--=P11V8_S0_NB_VCCD LVDS                                 14
--=P11V5_S0_NB_VCCD CRT                                  14
--P3V3_S0_NB_VCCA_CRTDAC                                 14
--=P3V3_S0_NB_VCCSYNC                                   14
--P11V5_S0_NB_VCCD_QDAC                                  14
--P3V3_S0_NB_VCCA_DAC_BG                                 14
--=GND NB VSSA_DAC_BG                                   14
--P3V3_S0_NB_VCCA_TVDSA                                  14
--P3V3_S0_NB_VCCA_TVDCB                                  14
--P3V3_S0_NB_VCCA_TVDAAC                                 14

```

15	<u>LVDS BKLT CTL</u>	—	NC LVDS BKLT CTL	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS BKLT EN</u>	—	NC LVDS BKLT_EN	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS VDD EN</u>	—	NC LVDS VDD EN	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS IBG</u>	—	NC LVDS IBG	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>TP LVDS VBG</u>	—	NC LVDS VBG	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A CLK N</u>	—	NC LVDS A CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A CLK P</u>	—	NC LVDS A CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B CLK N</u>	—	NC LVDS B CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B CLK P</u>	—	NC LVDS B CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A DATA N<0></u>	—	NC LVDS A DATAN<0>	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A DATA N<1></u>	—	NC LVDS A DATAN<1>	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A DATA N<2></u>	—	NC LVDS A DATAN<2>	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A DATA P<0></u>	—	NC LVDS A DATAP<0>	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A DATA P<1></u>	—	NC LVDS A DATAP<1>	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS A DATA P<2></u>	—	NC LVDS A DATAP<2>	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B DATA N<0></u>	—	NC LVDS B DATAN<0>	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B DATA N<1></u>	—	NC LVDS B DATAN<1>	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B DATA N<2></u>	—	NC LVDS B DATAN<2>	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B DATA P<0></u>	—	NC LVDS B DATAP<0>	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B DATA P<1></u>	—	NC LVDS B DATAP<1>	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>LVDS B DATA P<2></u>	—	NC LVDS B DATAP<2>	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>TP LVDS VREFH</u>	—	NC LVDS VREFH	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>TP LVDS VREFL</u>	—	NC LVDS VREFL	MAKE_BASE=TRUE NO_TEST=TRUE
15	<u>GFX VID<1></u>	—	TP GFX VID<1>	MAKE_BASE=TRUE
15	<u>GFX VID<2></u>	—	TP GFX VID<2>	MAKE_BASE=TRUE
15	<u>GFX VID<3></u>	—	TP GFX VID<3>	MAKE_BASE=TRUE
15	<u>GFX VID<4></u>	—	TP GFX VID<4>	MAKE_BASE=TRUE
15	<u>=GFX VR EN</u>	—	TP GFX VR EN	MAKE_BASE=TRUE

NB Graphics Decoupling

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

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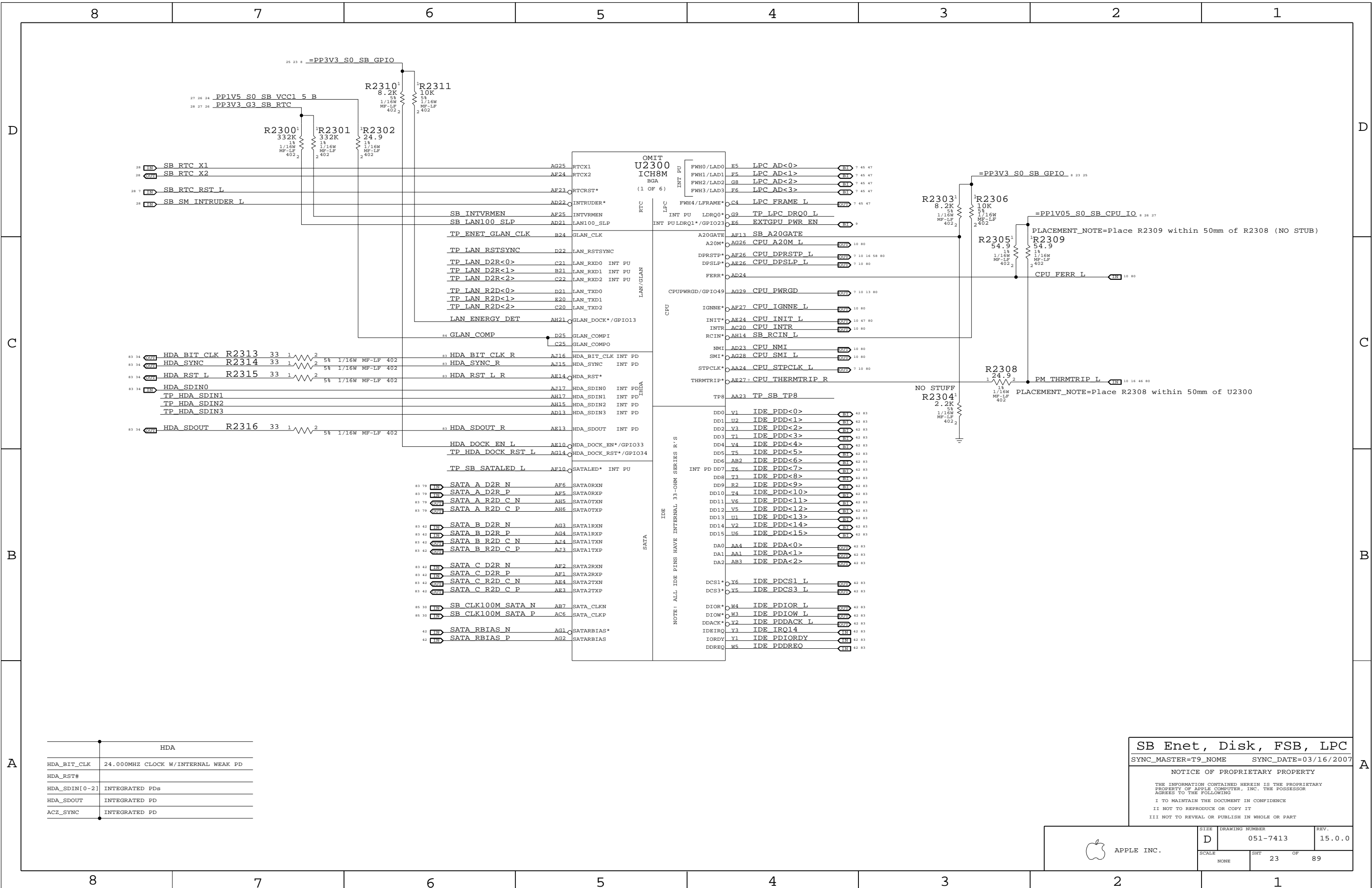
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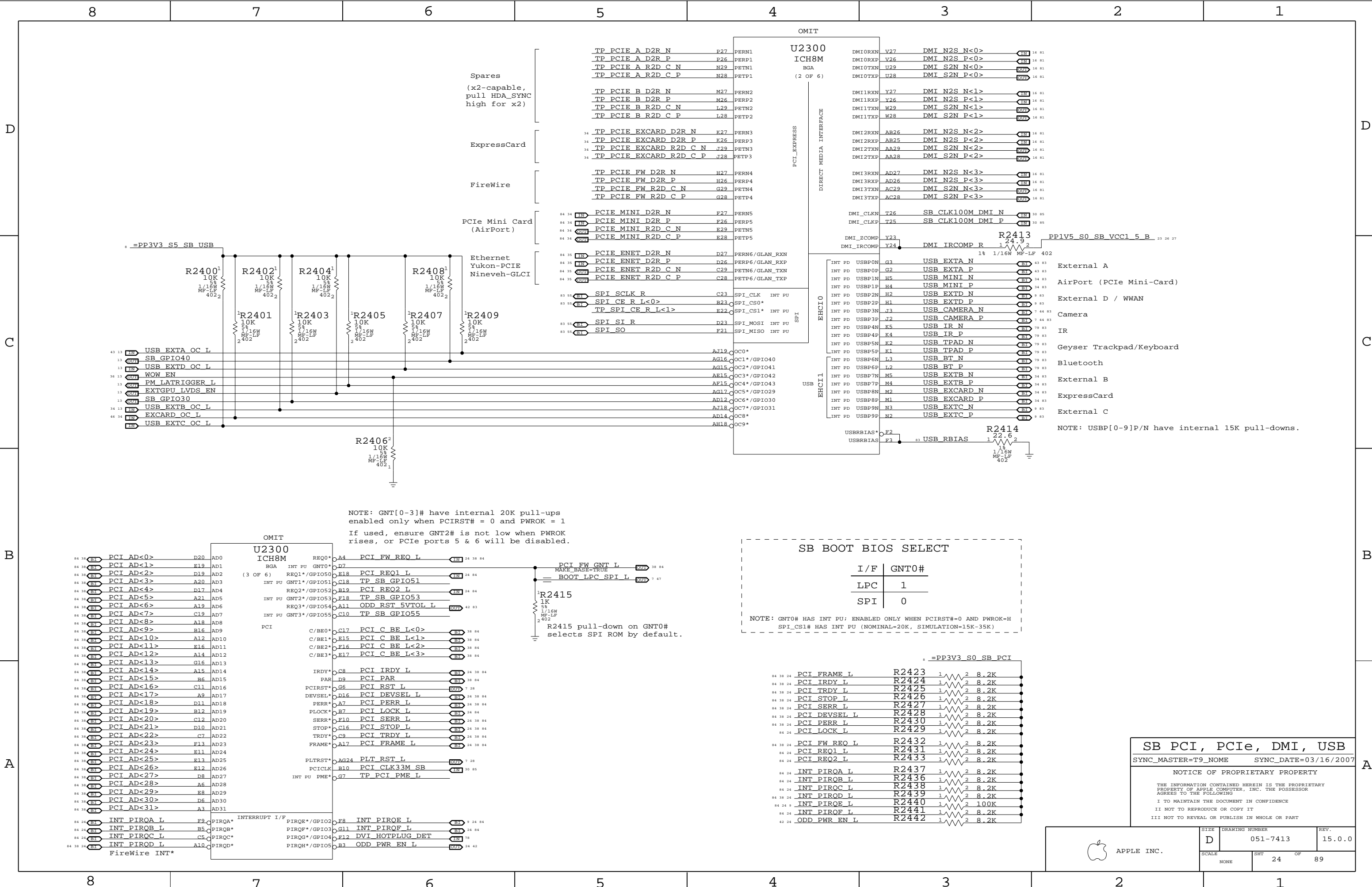
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SIZE D	DRAWING NUMBER 051-7413	REV. 15.0.0
SCALE AS SHOWN	SHT 22 OF 89	

Current numbers from Crestline EDS Addendum, doc #20127





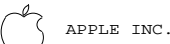
NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1
If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.

SB BOOT BIOS SELECT		
I/F	GNT0#	
LPC	1	
SPI	0	

NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

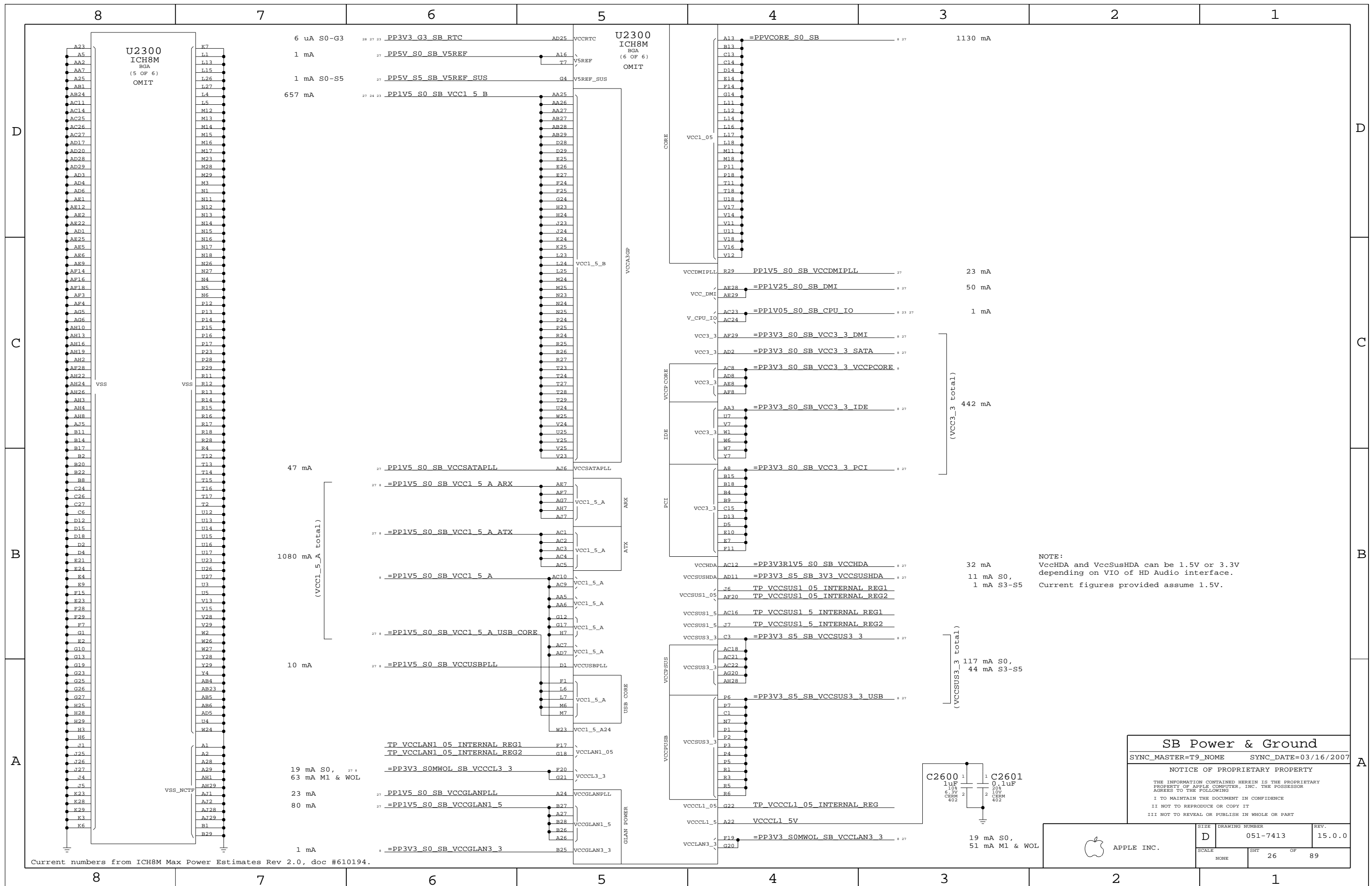
SB PCI, PCIe, DMI, USB
SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

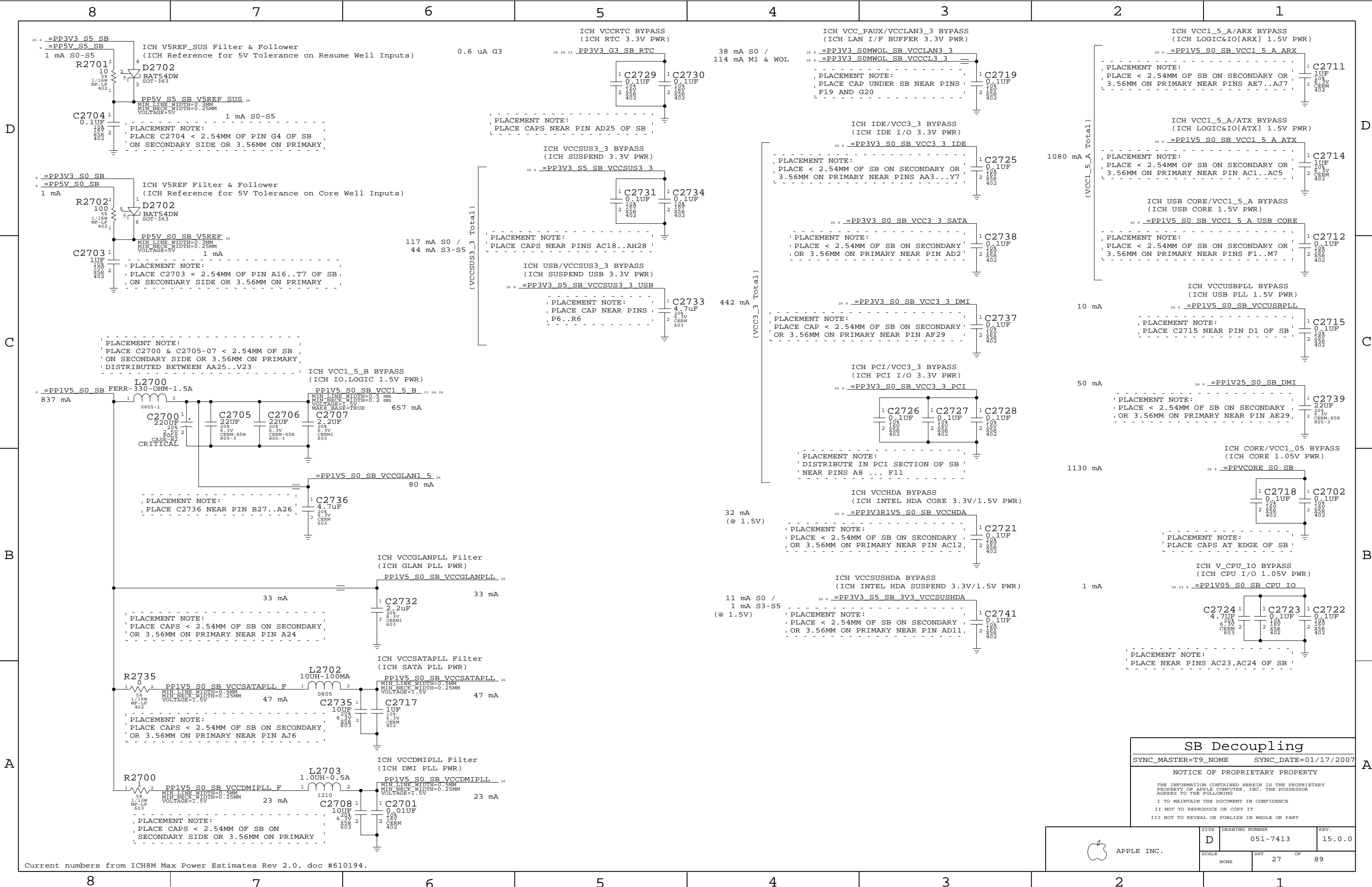
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SCALE	SHT	OF
NONE	24	89





SB Decoupling

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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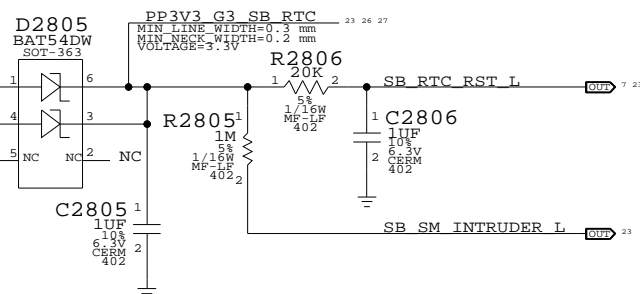
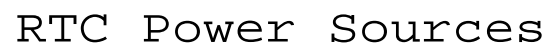
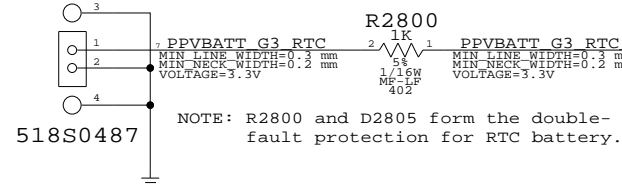
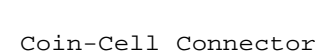
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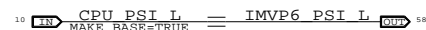
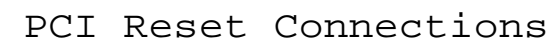
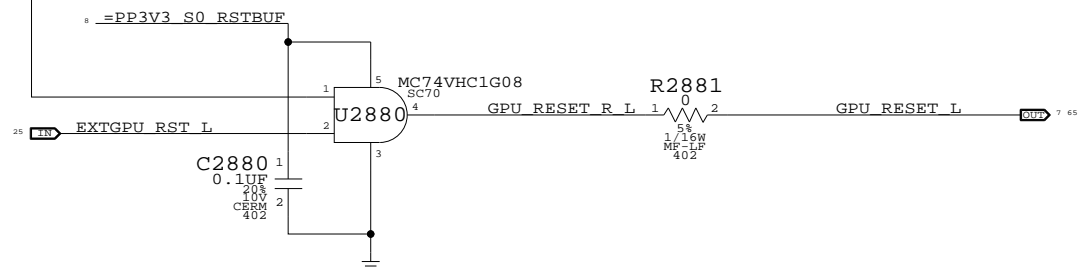
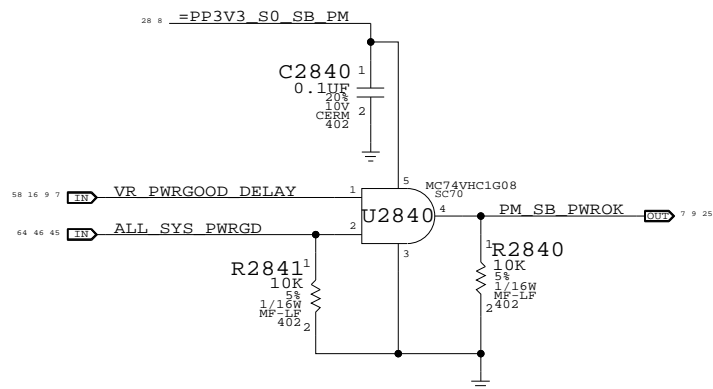
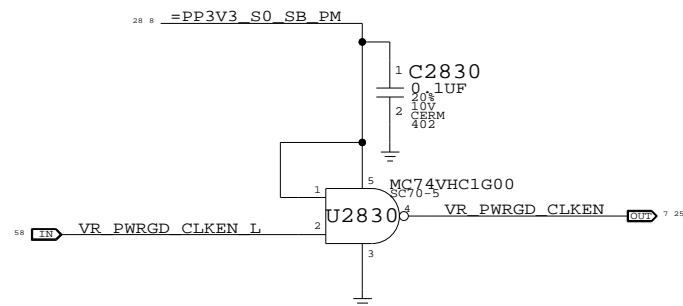
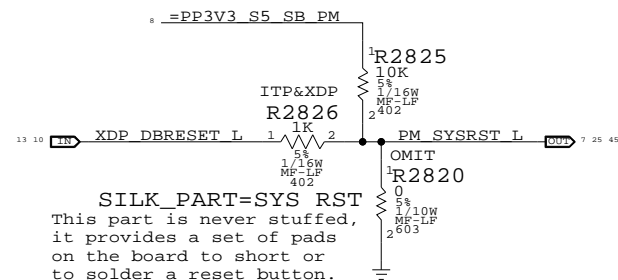
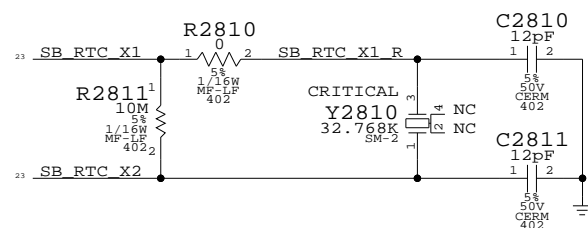
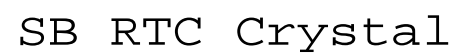
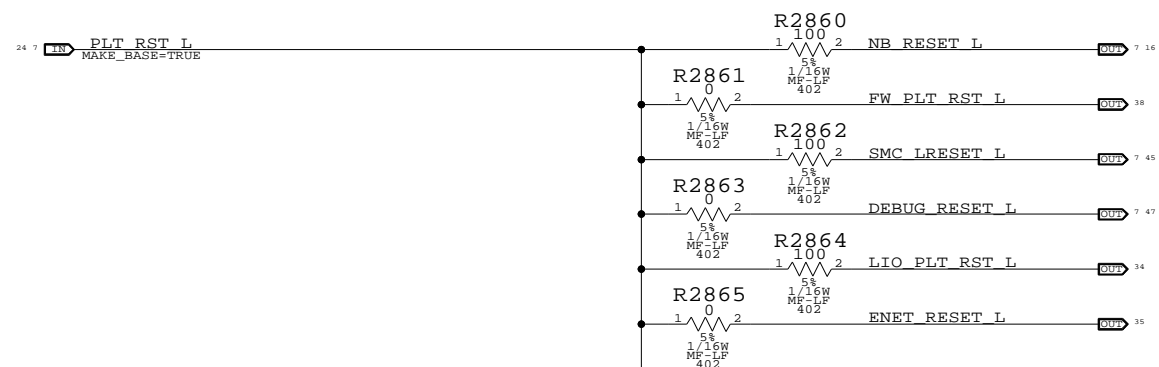
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	D	051-7413	15.0.0
	SCALE	SHT	OF
	NONE	27	89



Unbuffered



SB Misc

SYNC_MASTER= (T9_MLB)	SYNC_DATE=08/24/2006
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SIZE	D
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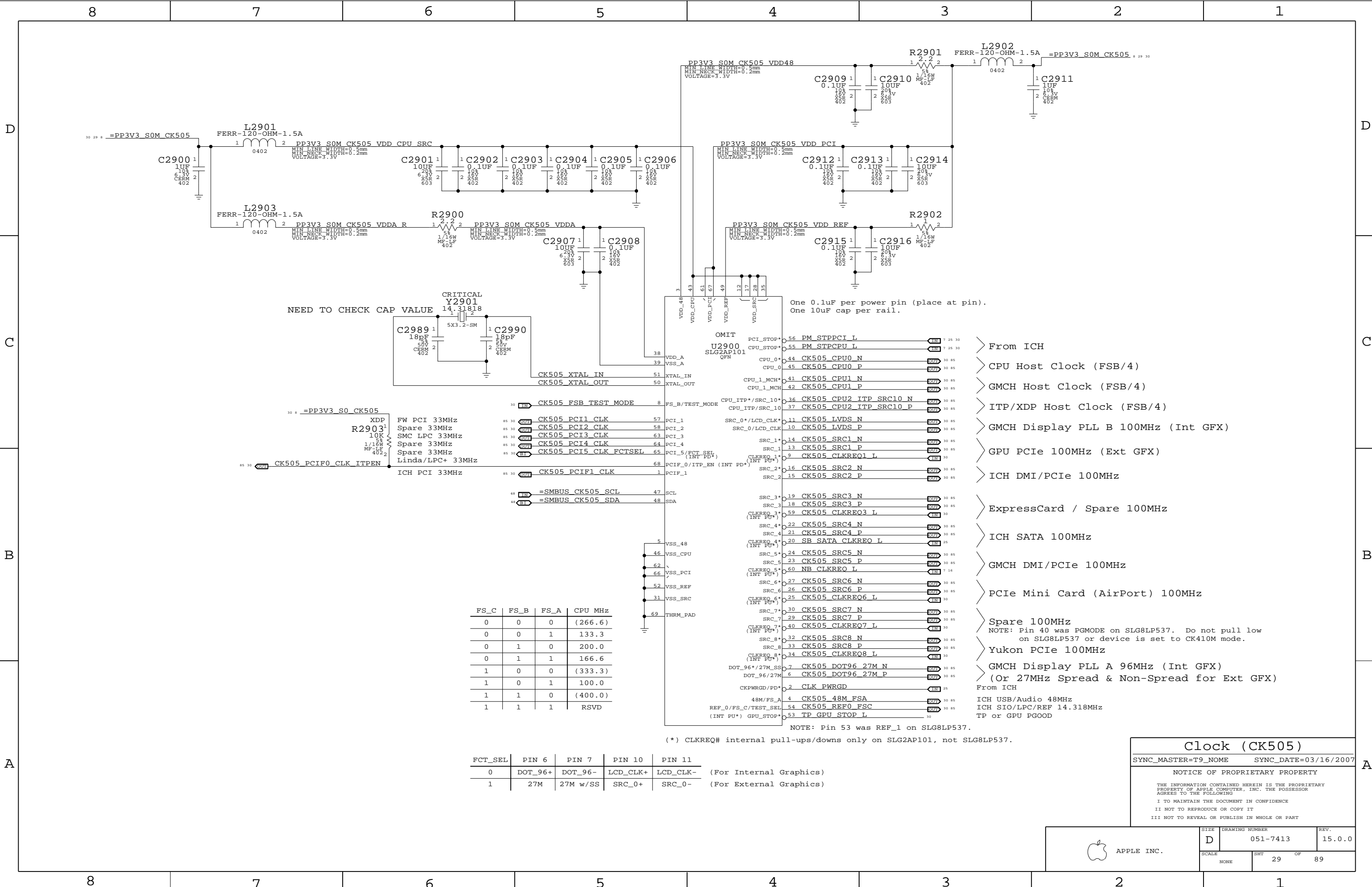
SIZE	DRAWING NUMBER
D	051-

REV.	15.0.0
------	--------

SCALE	NO
-------	----

SHT	
-----	--

28



One 0.1uF per power pin (place at pin).
One 10uF cap per rail.

- > From ICH
 - > CPU Host Clock (FSB/4)
 - > GMCH Host Clock (FSB/4)
 - > ITP/XDP Host Clock (FSB/4)
 - > GMCH Display PLL B 100MHz (Int GFX)
 - > GPU PCIe 100MHz (Ext GFX)
 - > ICH DMI/PCIe 100MHz
 - > ExpressCard / Spare 100MHz
 - > ICH SATA 100MHz
 - > GMCH DMI/PCIe 100MHz
 - > PCIe Mini Card (AirPort) 100MHz
 - > Spare 100MHz
NOTE: Pin 40 was PGMODE on SLG8LP537. Do not pull low on SLG8LP537 or device is set to CK410M mode.
 - > Yukon PCIe 100MHz
 - > GMCH Display PLL A 96MHz (Int GFX)
(Or 27MHz Spread & Non-Spread for Ext GFX)
- From ICH
- ICH USB/Audio 48MHz
 - ICH SIO/LPC/REF 14.318MHz
 - TP or GPU PGOOD

NOTE: Pin 53 was REF_1 on SLG8LP537.

(*) CLKREQ# internal pull-ups/downs only on SLG2AP101, not SLG8LP537.

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

Clock (CK505)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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SIZE
D

DRAWING NUMBER
051-7413

REV.
15.0.0

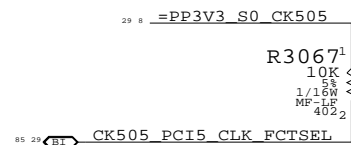
SCALE
NONE

SHT
29

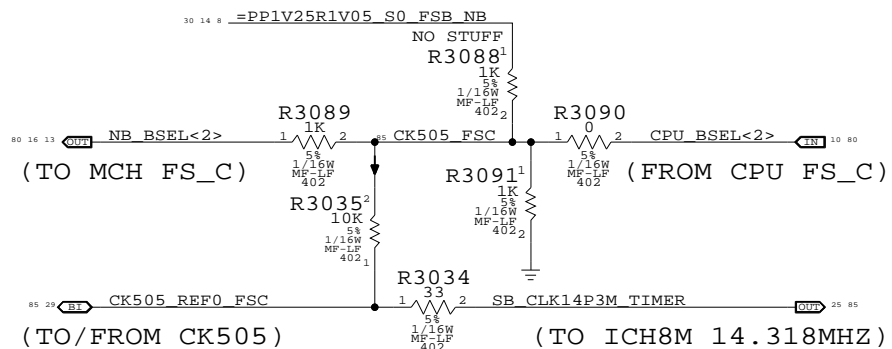
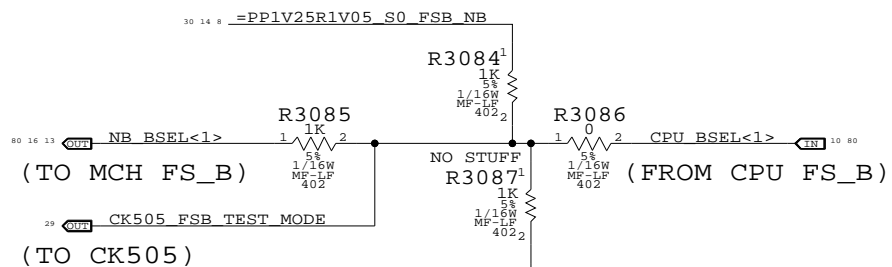
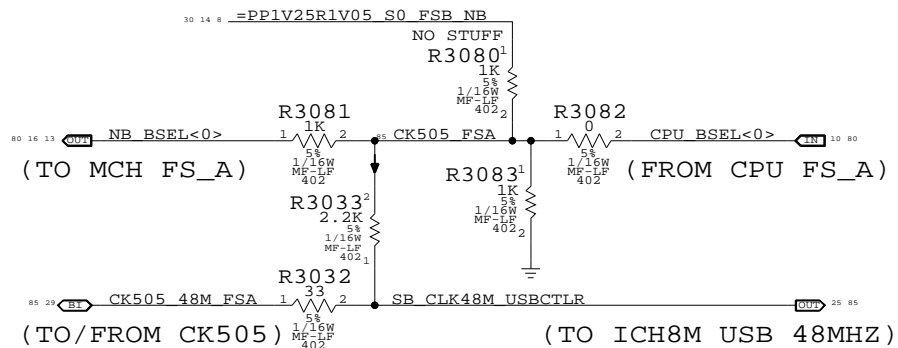
OF
89

CK505 Configuration Straps

FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)



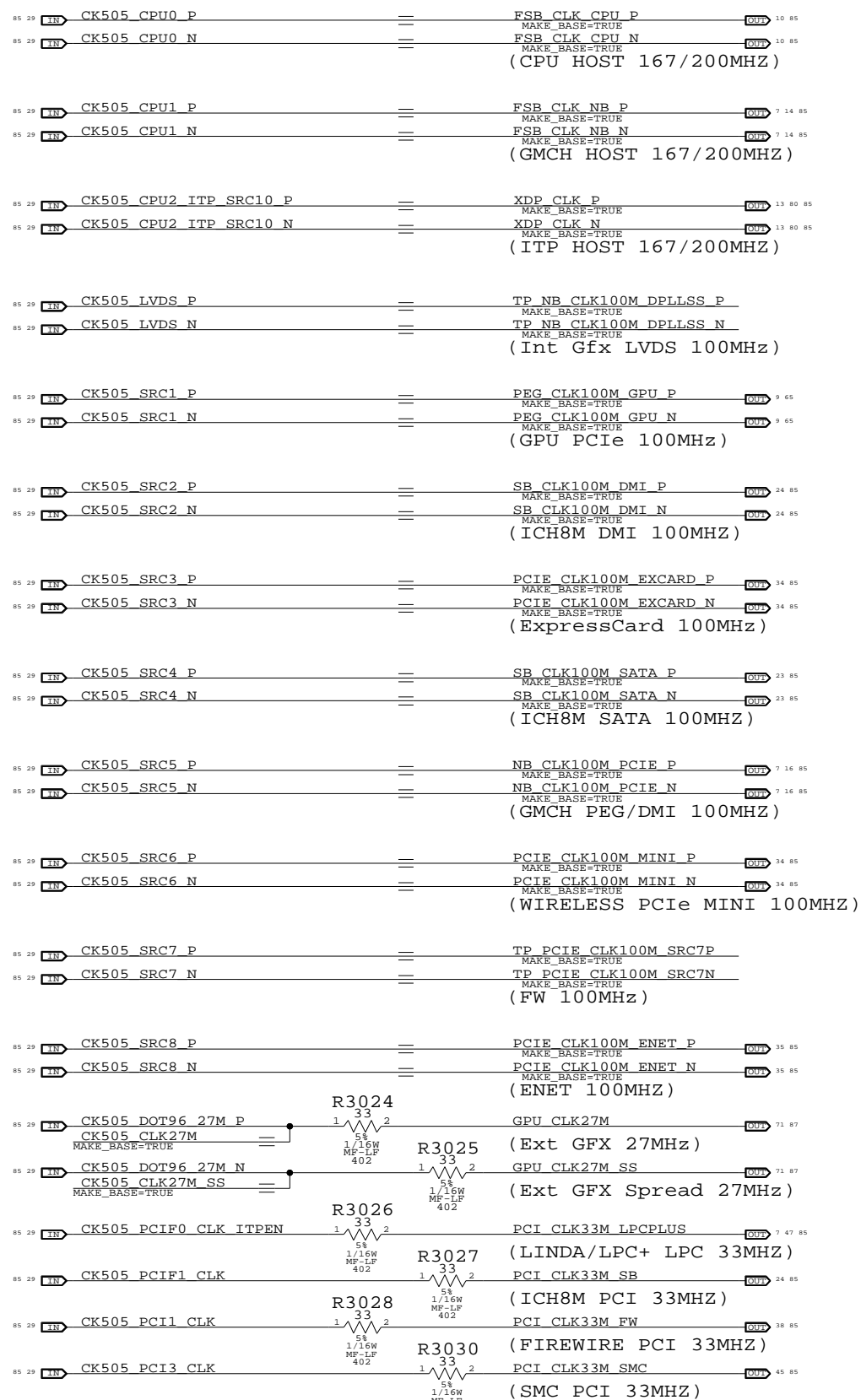
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090
for manual CPU clk frequency.

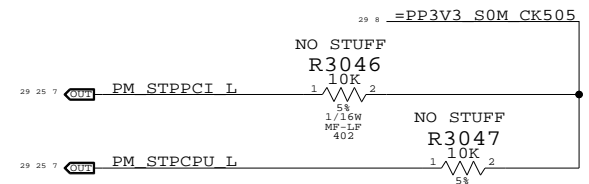
(Only 100-200MHz supported by
SLG8LP536 and CY28545-5)

CLK Termination

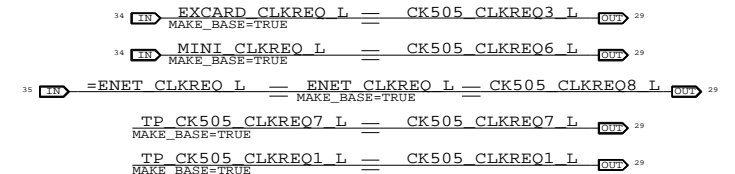
(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)



CLKREQ Controls



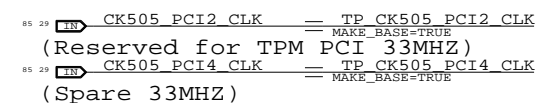
Silego SLG2AP101 has internal pull-ups⁴⁰² on all CLKRE# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).



GPU Clock Gating



Unused Clocks



Clock Termination

SYNC_MASTER=(MASTER)	SYNC_DATE=08/23/2006	7
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SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	30	89

Page Notes

Power aliases required by this page:

- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

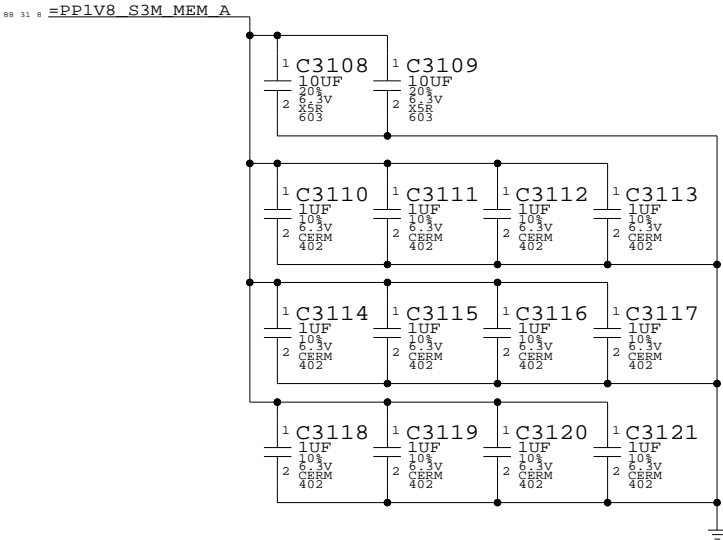
BOM options provided by this page:

(NONE)

"Factory" (thru-hole) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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SIZE

D

DRAWING NUMBER

051-7413

REV.

15.0.0

SCALE

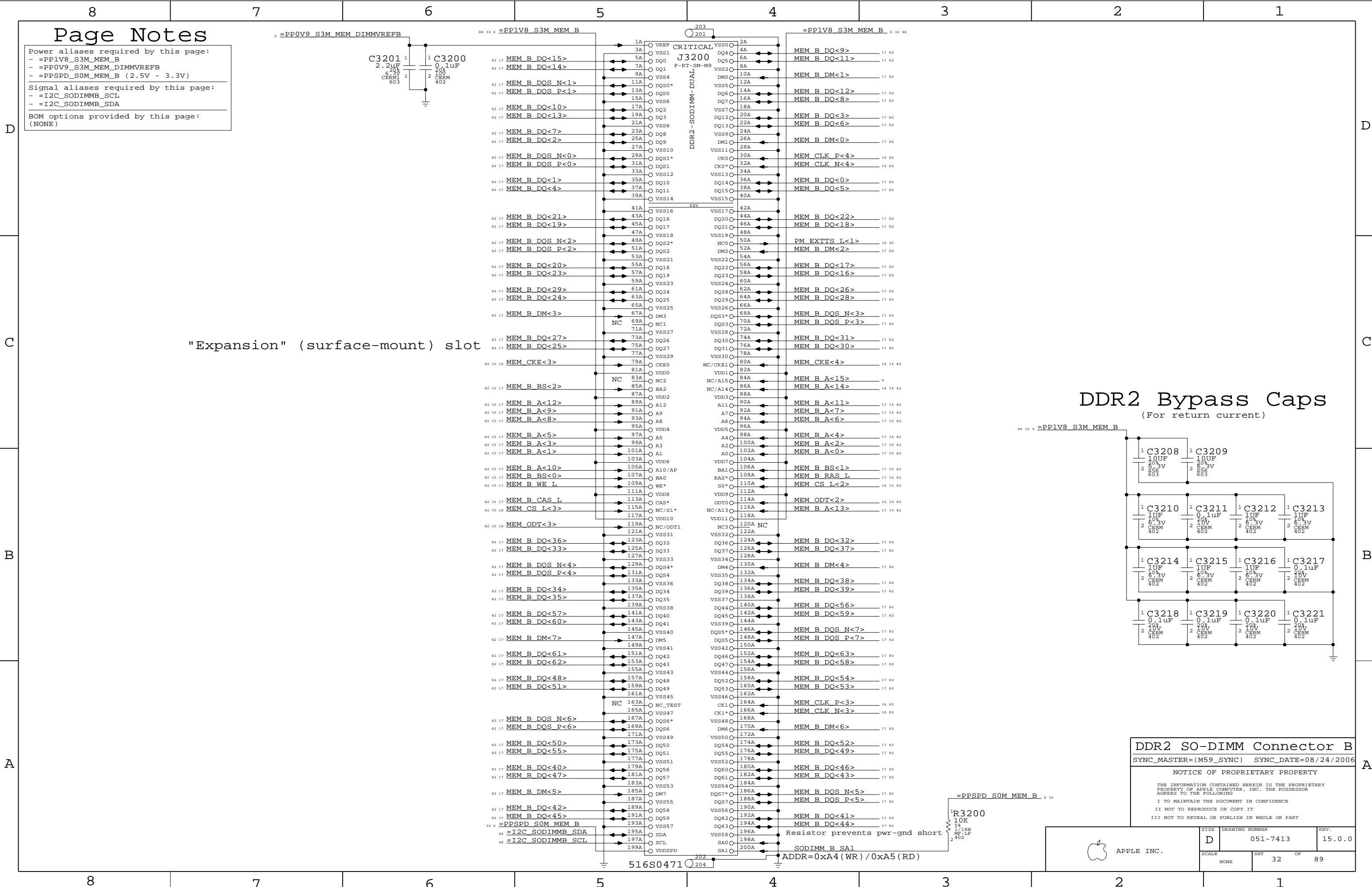
NONE

SHT

31

OF

89



Page Notes

Power aliases required by this page:
- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

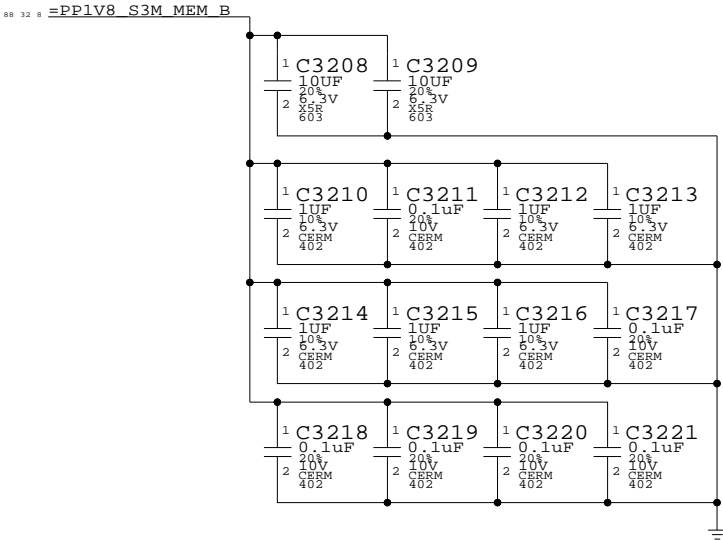
Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

"Expansion" (surface-mount) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B
SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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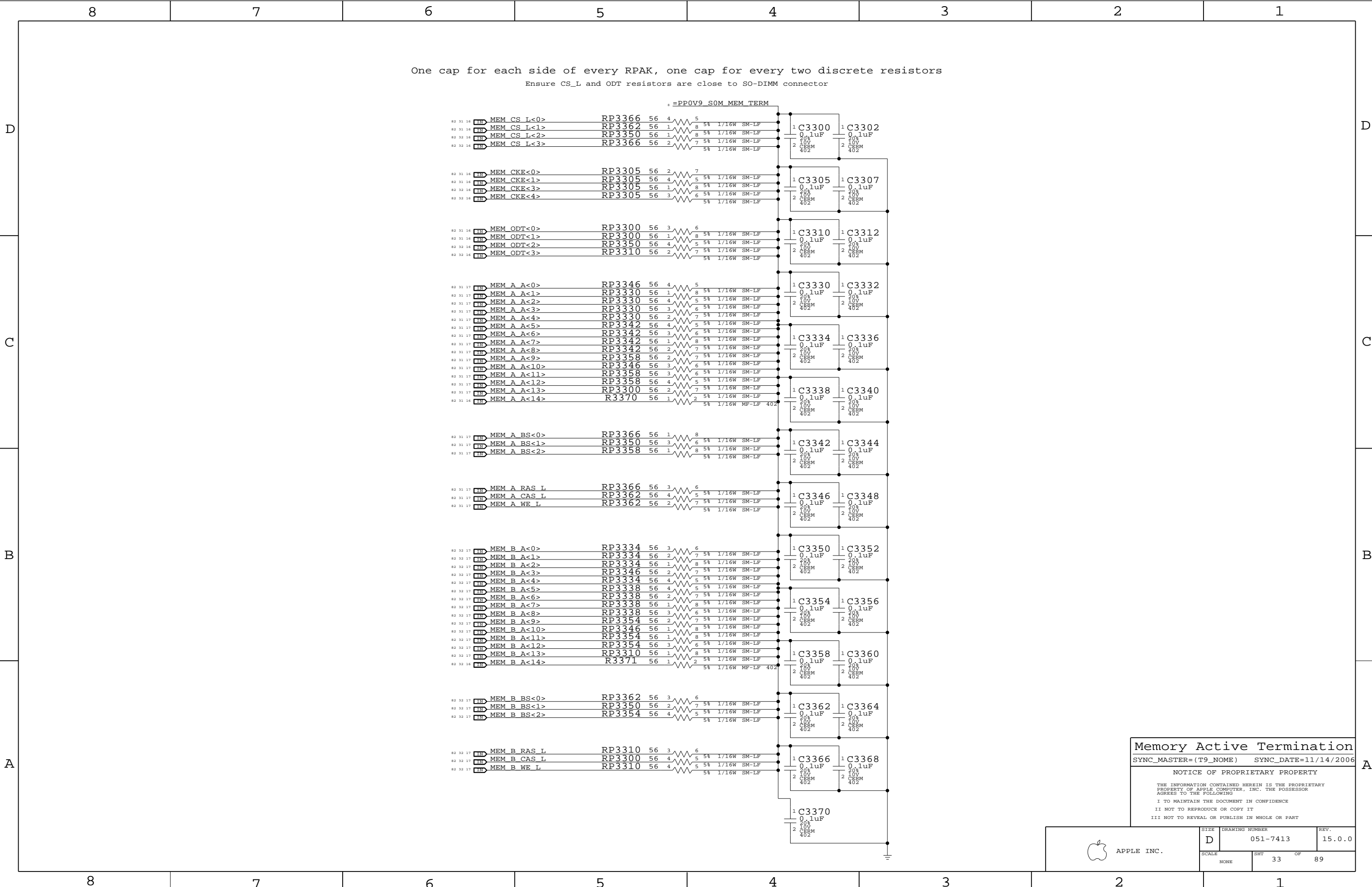
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SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	32	89



Memory Active Termination

SYNC_MASTER=(T9_NOME) SYNC_DATE=11/14/2006

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SIZE

D

DRAWING NUMBER

051-7413

REV.

15.0.0

SCALE

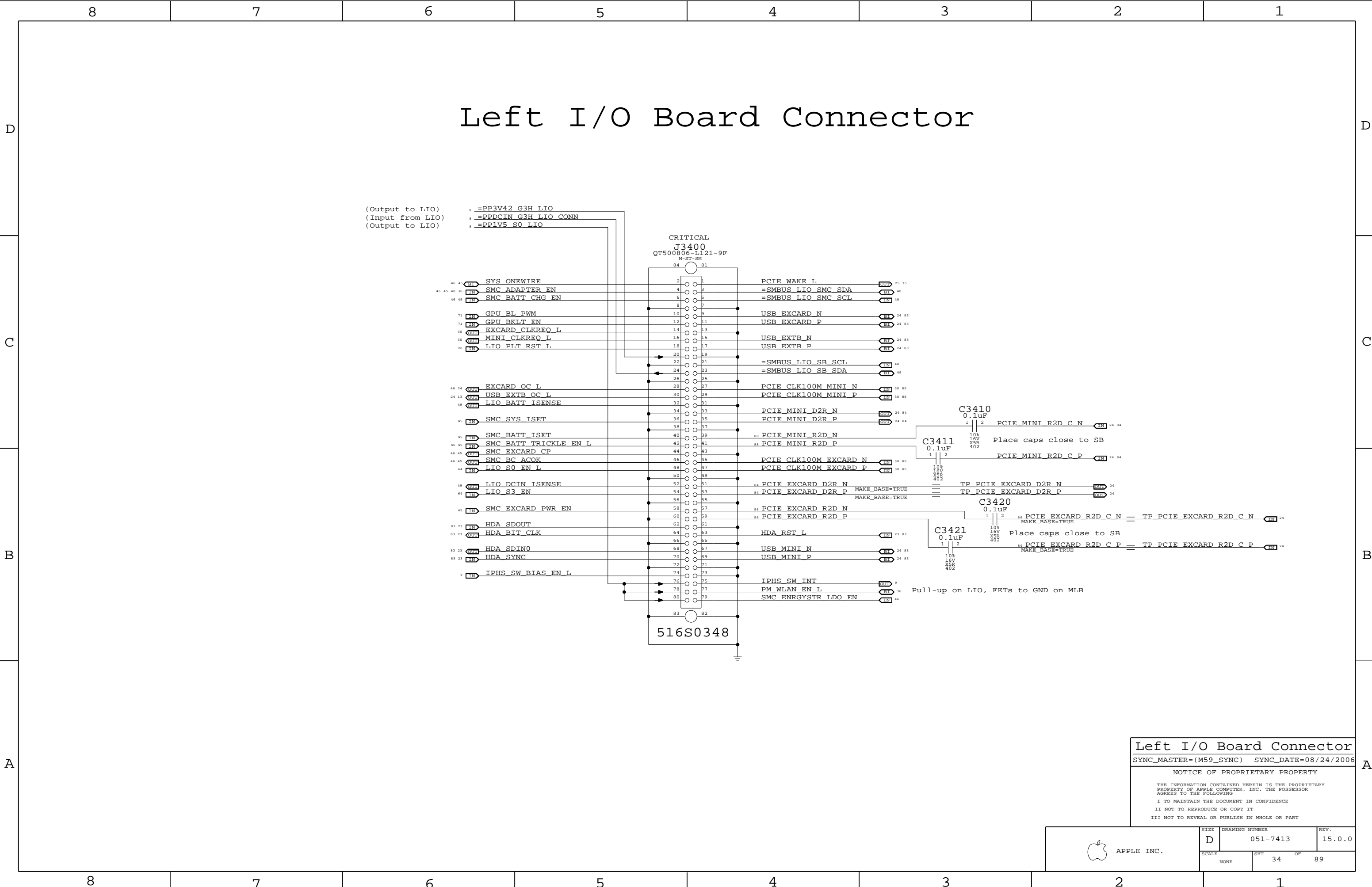
NONE

SHT

33

OF

89



Left I/O Board Connector

(Output to LIO)
(Input from LIO)
(Output to LIO)

=PP3V42_G3H_LIO
=PPDCIN_G3H_LIO_CONN
=PP1V5_S0_LIO

CRITICAL
J3400
QT500806-L121-9F
M-ST-SM

516S0348

Pull-up on LIO, FETs to GND on MLB

Left I/O Board Connector

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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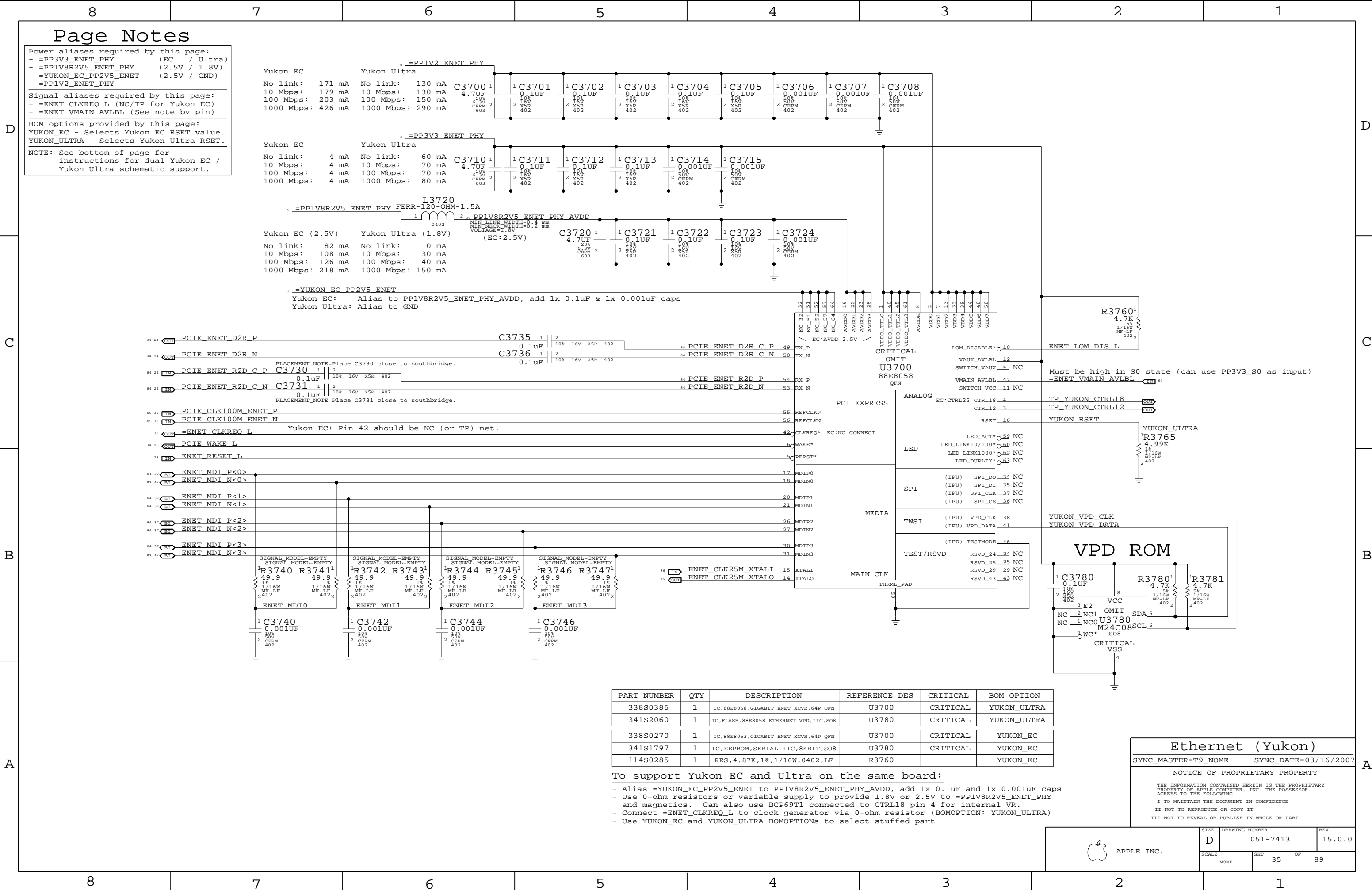
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SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	34	89



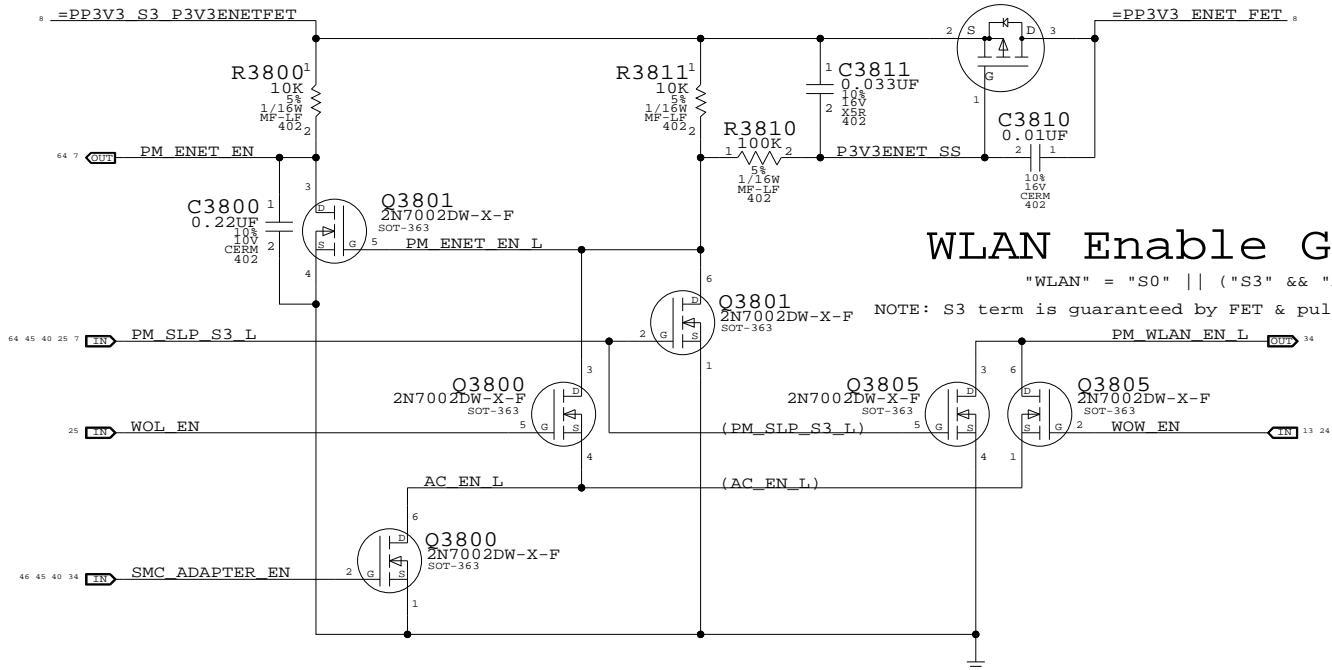
To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

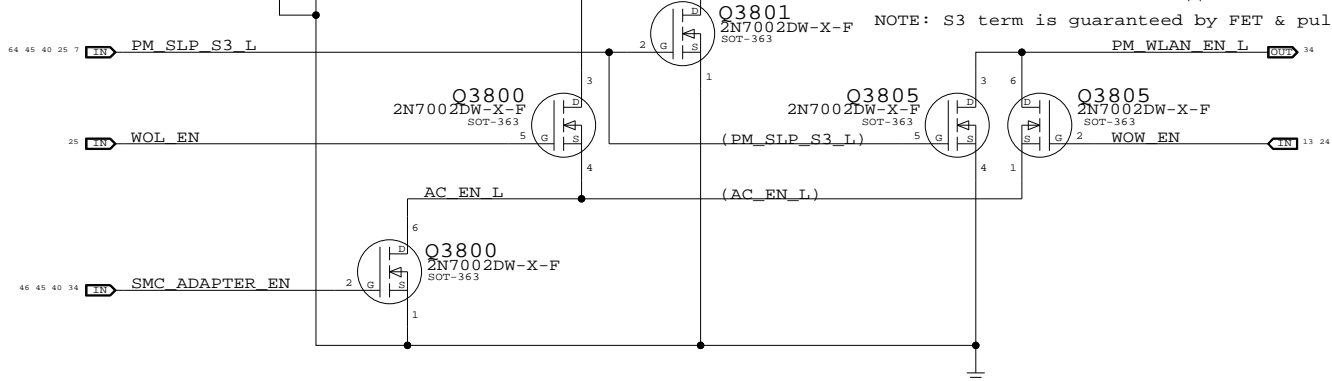


3.3V ENET FET

WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")

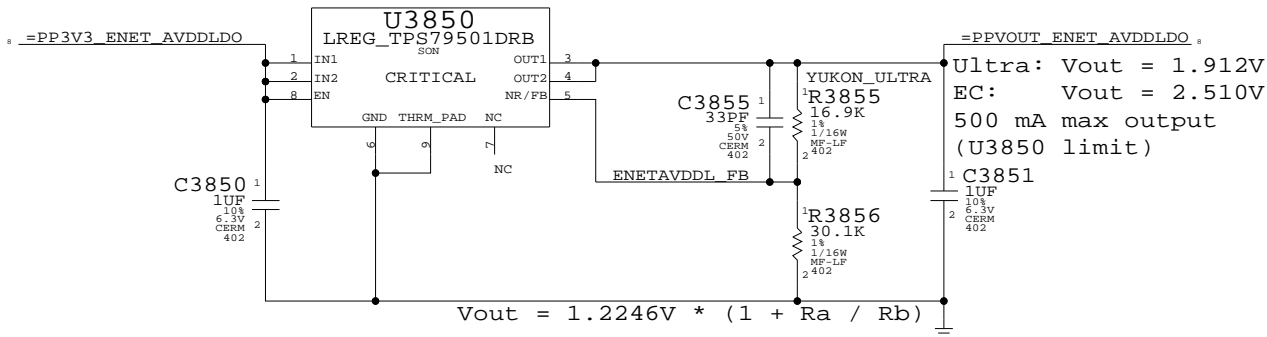
NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.



Yukon AVDDL LDO

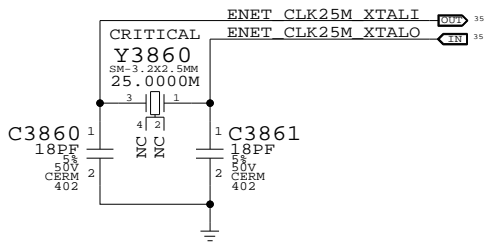
1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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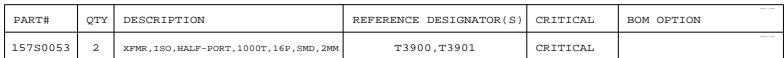
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SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	36	89

Power aliases required by this page:
=GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

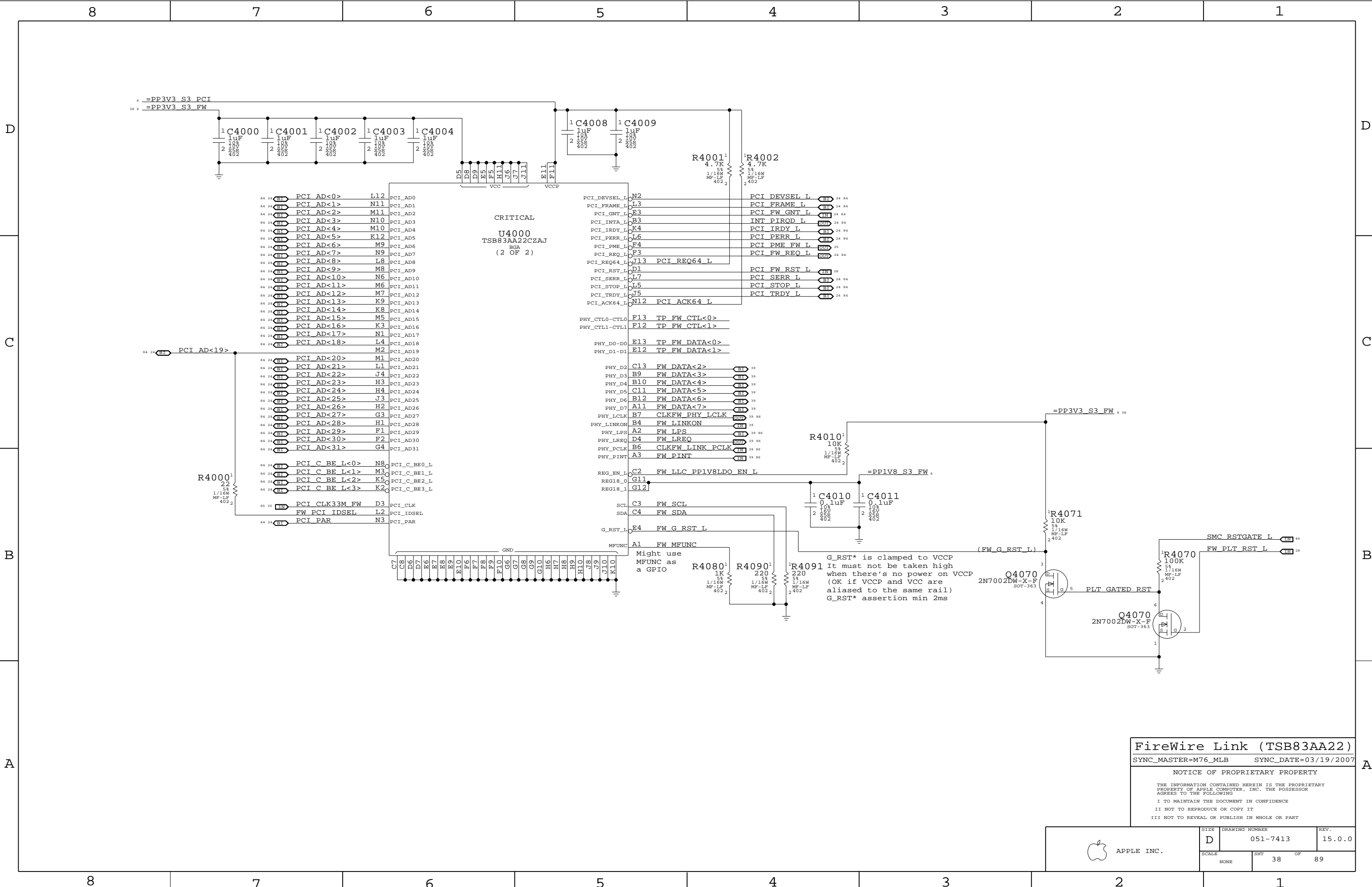


Ethernet Connector	
SYNC_MASTER=M76_MLB	SYNC_DATE=03/19/2007
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SIZE D	DRAWING NUMBER 051-7413	REV. 15.0.0
SCALE NONE	SHT 37	OF 89



FireWire Link (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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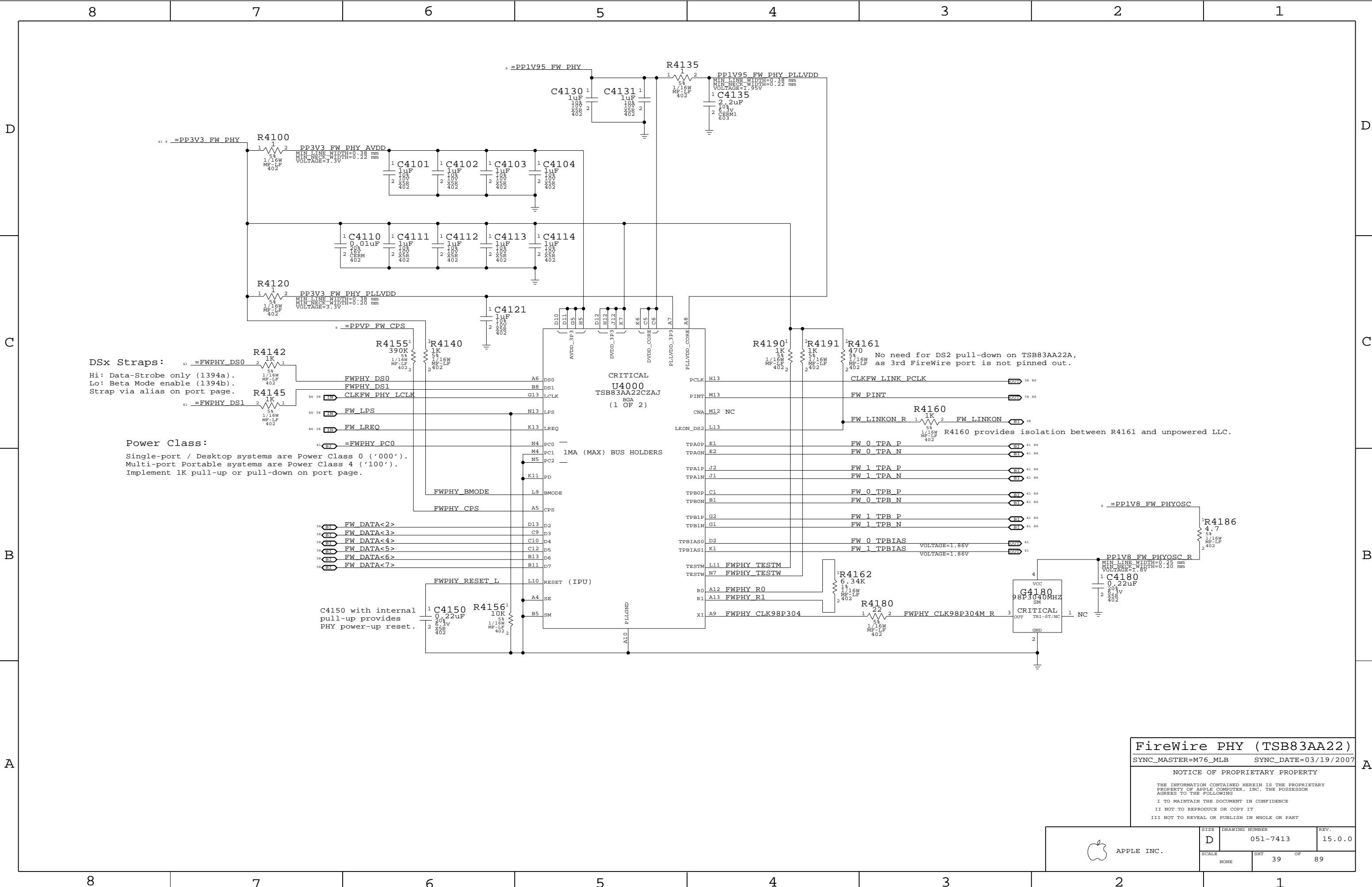
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SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	38	89



FireWire PHY (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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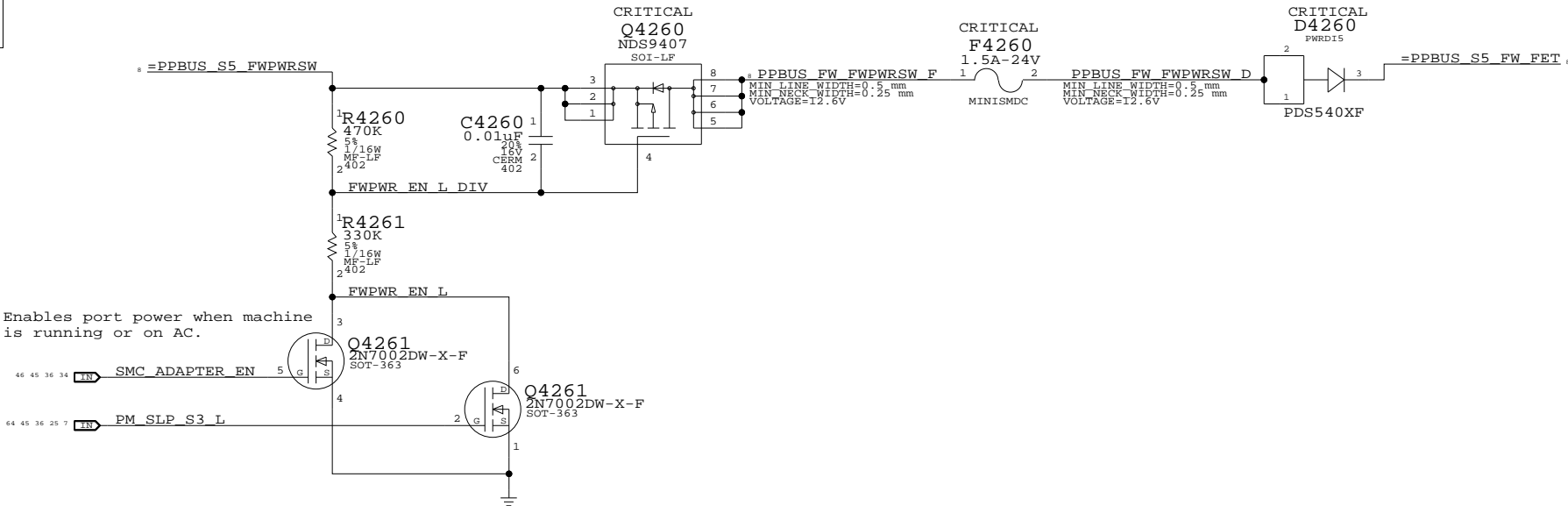
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	39	89

Page Notes

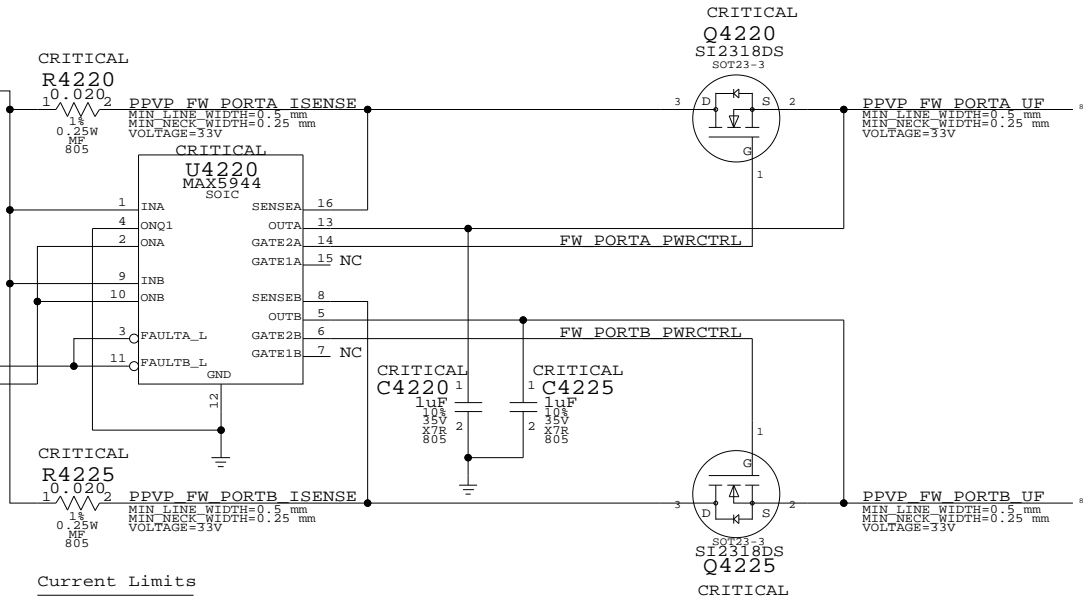
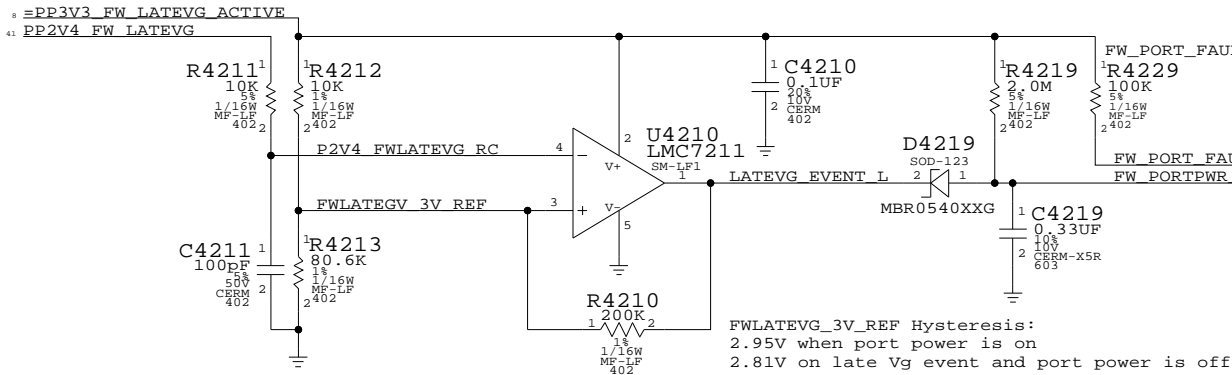
Power aliases required by this page:
- =PPBUS_S5_FWPWSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch



Current Limit/Active Late-VG Protection

Late-VG Event Detection



Current Limits
0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

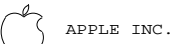
MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

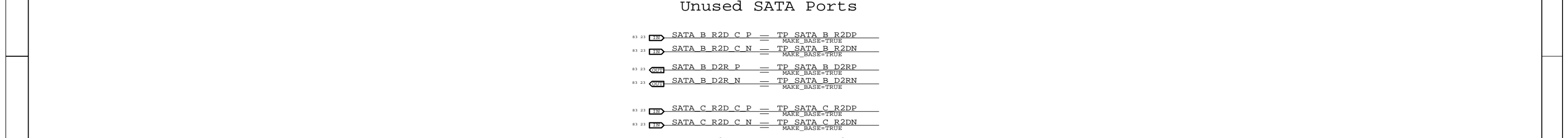
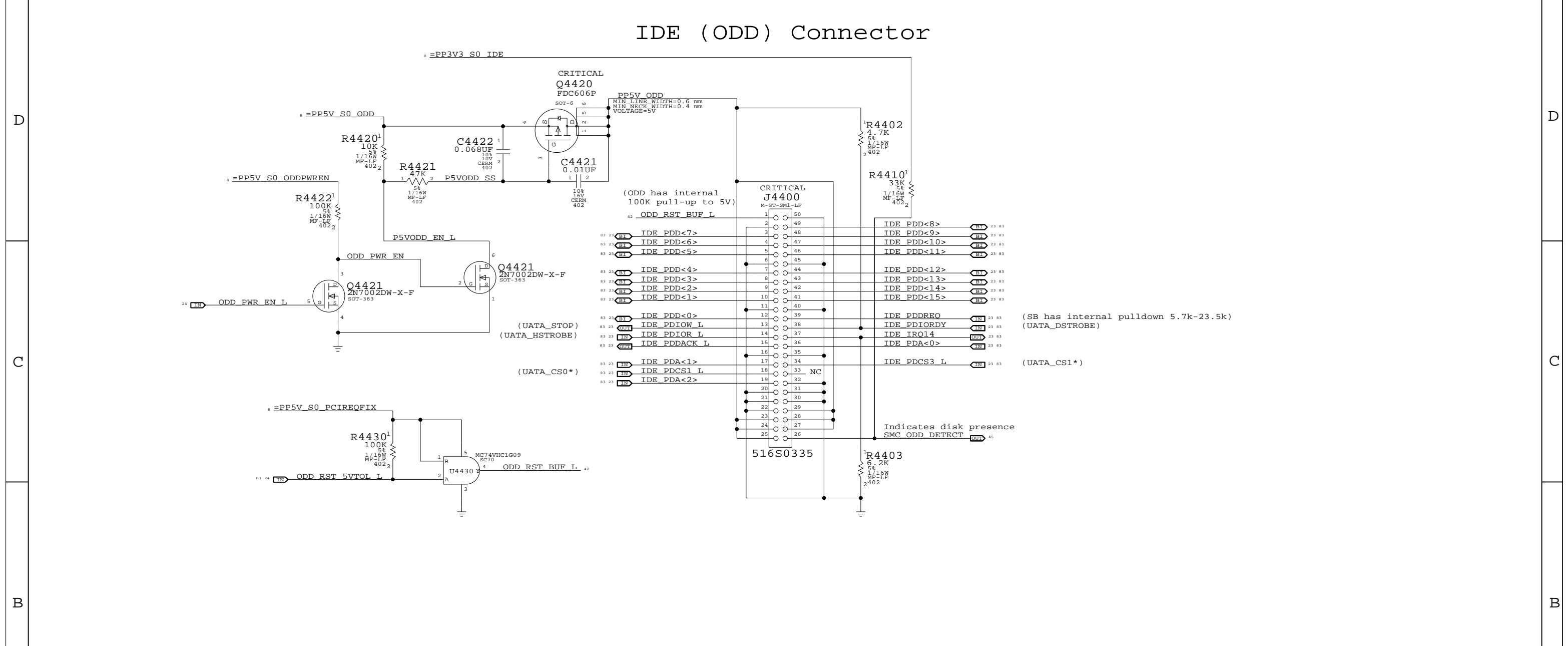
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SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	40	89

8	7	6	5	4	3	2	1
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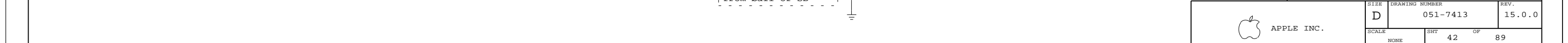



A

Placement note
Place within 12.7mm
1/16W
MP-LP
from ball of SB
2 402

PATA Connector	
SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
NOTICE OF PROPRIETARY PROPERTY	
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A



<div style="text-align: center;"> <h1>PATA Connector</h1> <p> SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER) </p> <p style="text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p> THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING </p> <p>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p>II NOT TO REPRODUCE OR COPY IT</p> <p>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> </div>			
 <p>APPLE INC.</p>	SIZE	DRAWING NUMBER	REV.
	D	051-7413	15.0.0
	SCALE	SHT	OF
	NONE	42	89


SINE_WINDOW=(WINDOW)	SINE_SIZE=(WINDOW)	A

NOTICE OF PROPRIETARY PROPERTY

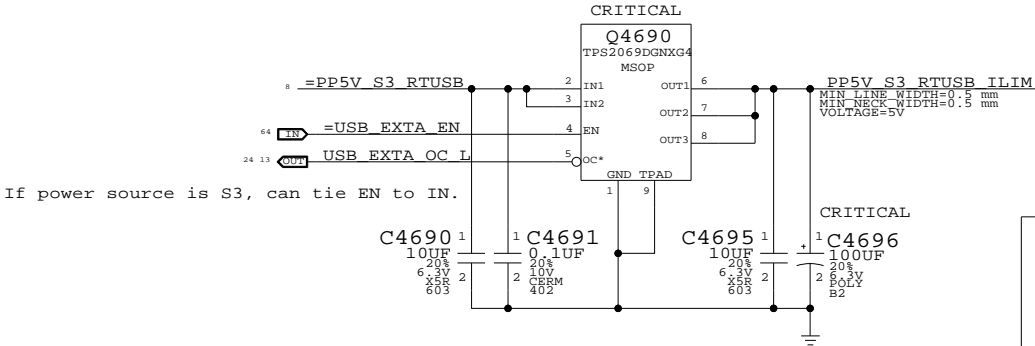
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	II NOT TO REPRODUCE OR COPY IT	
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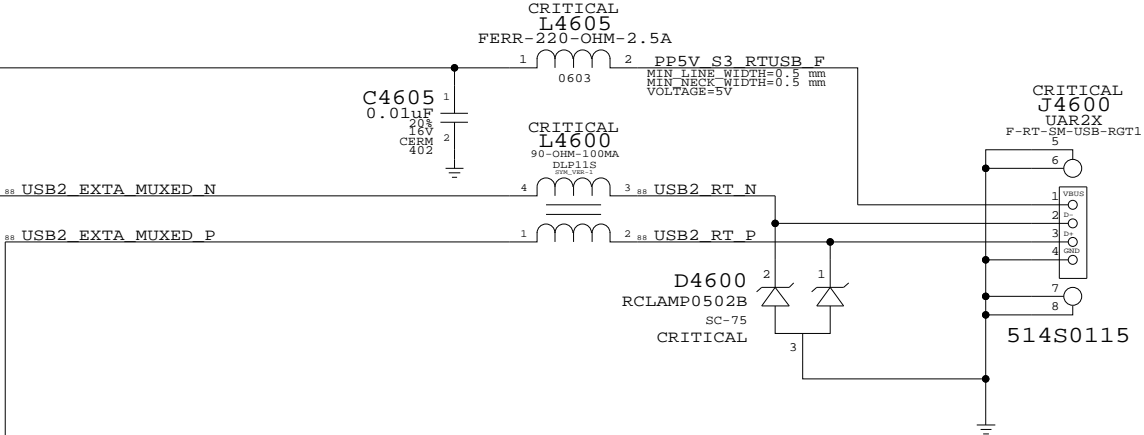
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	15.0.0
	SCALE	SHT	OF
	NONE	42	89

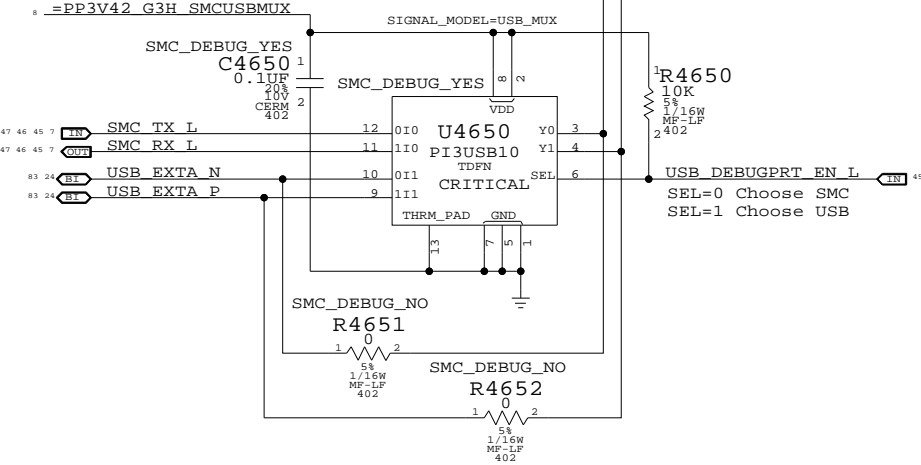
Port Power Switch



Right USB Port



USB/SMC Debug Mux



External USB Connector

SYNC_MASTER=M88 SYNC_DATE=08/02/2007

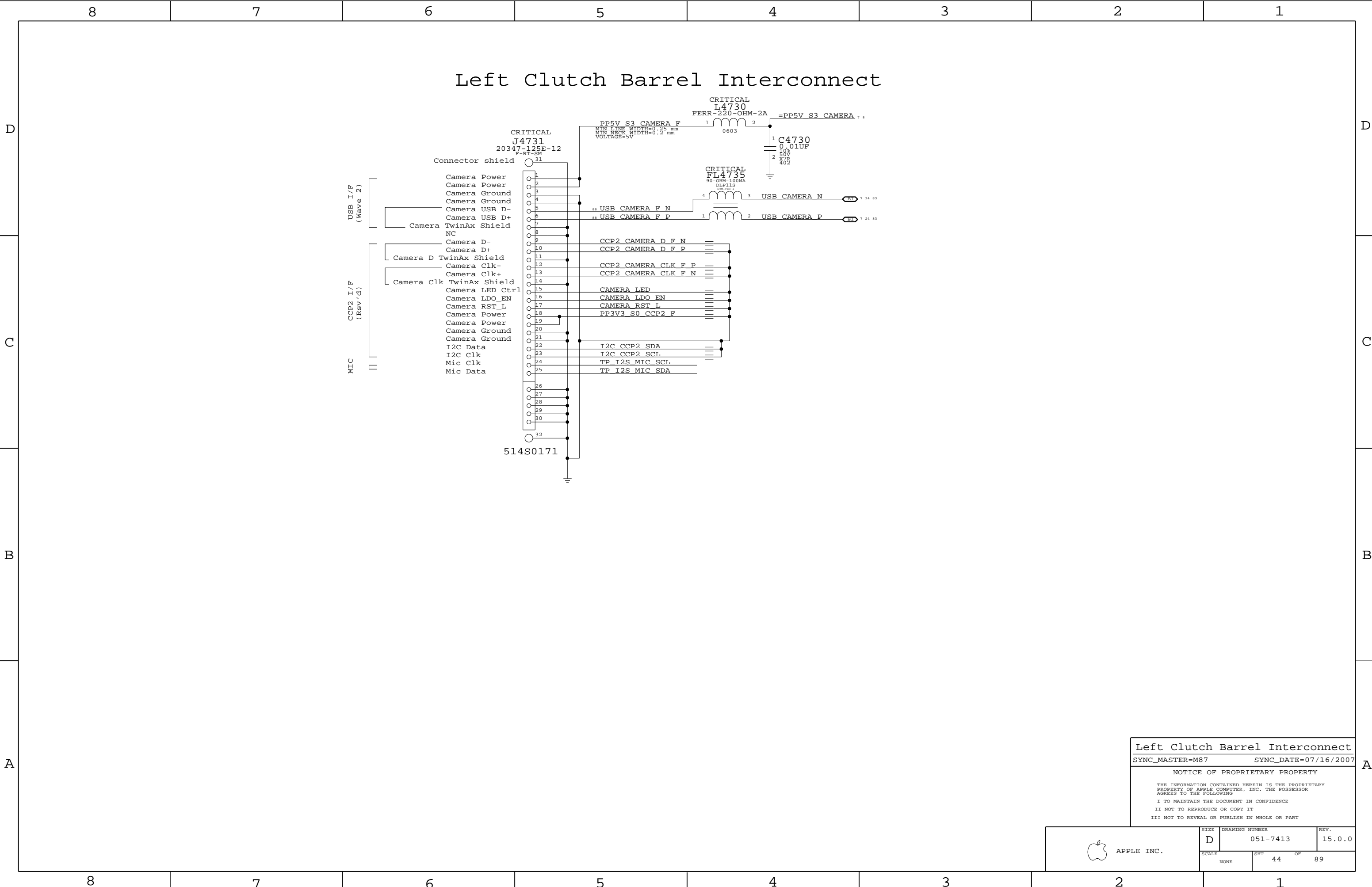
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SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	43	89



Left Clutch Barrel Interconnect

SYNC_MASTER=M87 SYNC_DATE=07/16/2007

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7413

REV.

15.0.0

SCALE

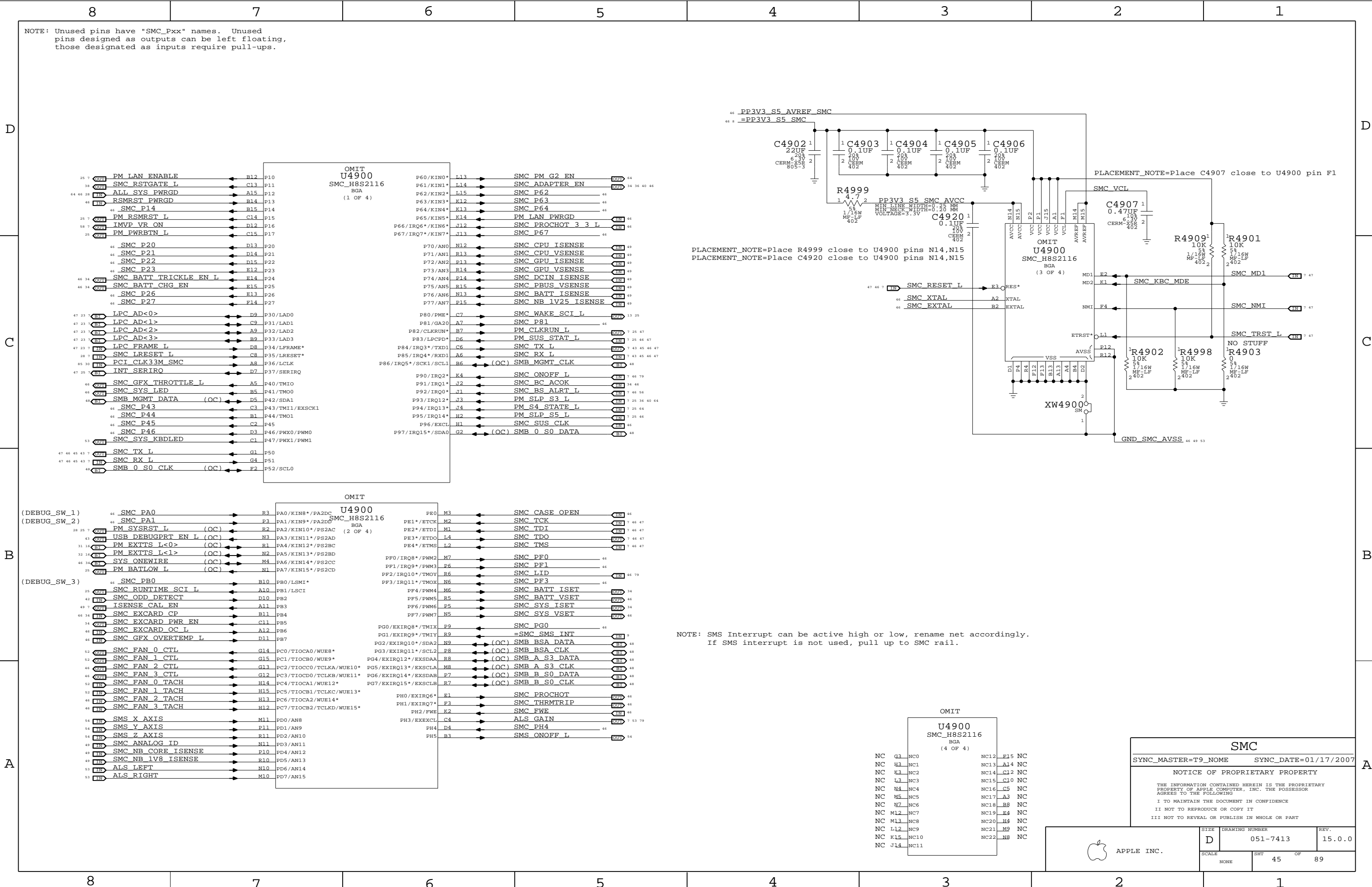
NONE

SHT

44

OF

89




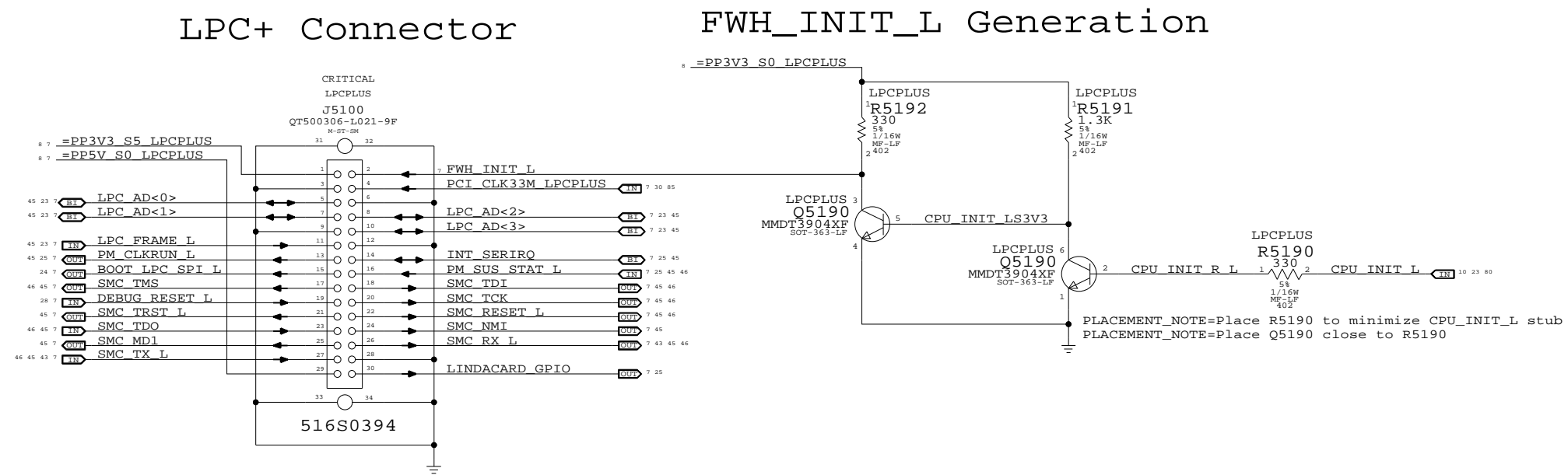
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B



 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	15.0.0
	SCALE	SHT	OF
	NONE	46	89




(TC0D)

(Th2H)
(Reserved for CPU heatpipe sensor)

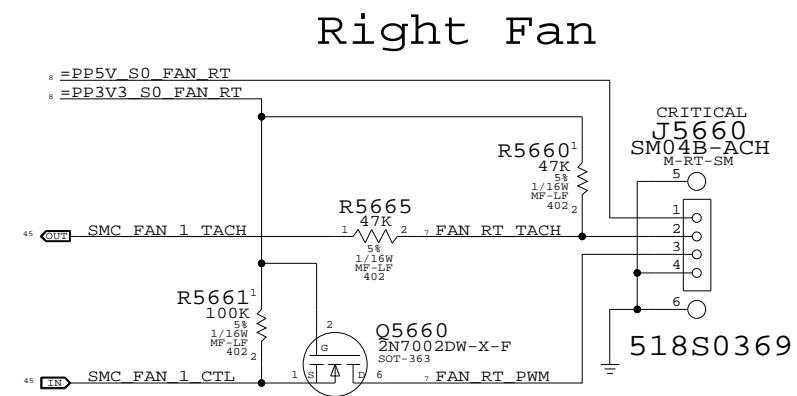
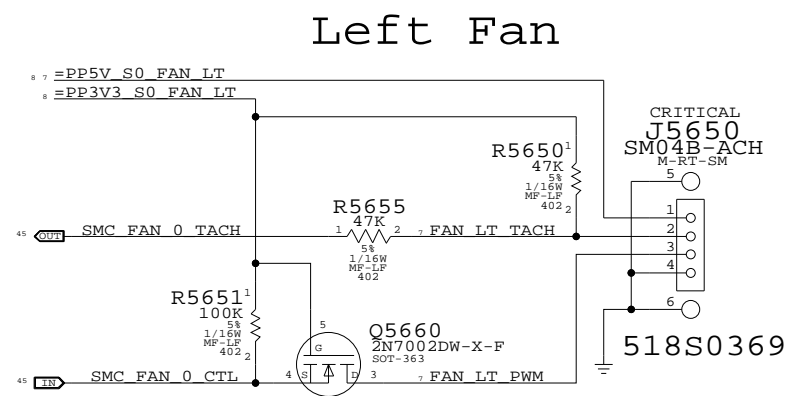
518S0487

NB Thermal Diodes Not Used

[illegible]

 APPLE INC.	SIZE D	DRAWING NUMBER 051-7413	REV. 15.0.0
	SCALE NONE	SHT 51	OF 89





Fan Connectors

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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APPLE INC.

SIZE
D

SIZE	DRAWING NUMBER
------	----------------

DATE	DRAWING NUMBER
D	051-7413

15.0.0

SCALE	

NONE

SHT	5.0
-----	-----

52

22

89

1

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1

D



D



B



ALS Support

APPLE INC.

SIZE
D

051-7413

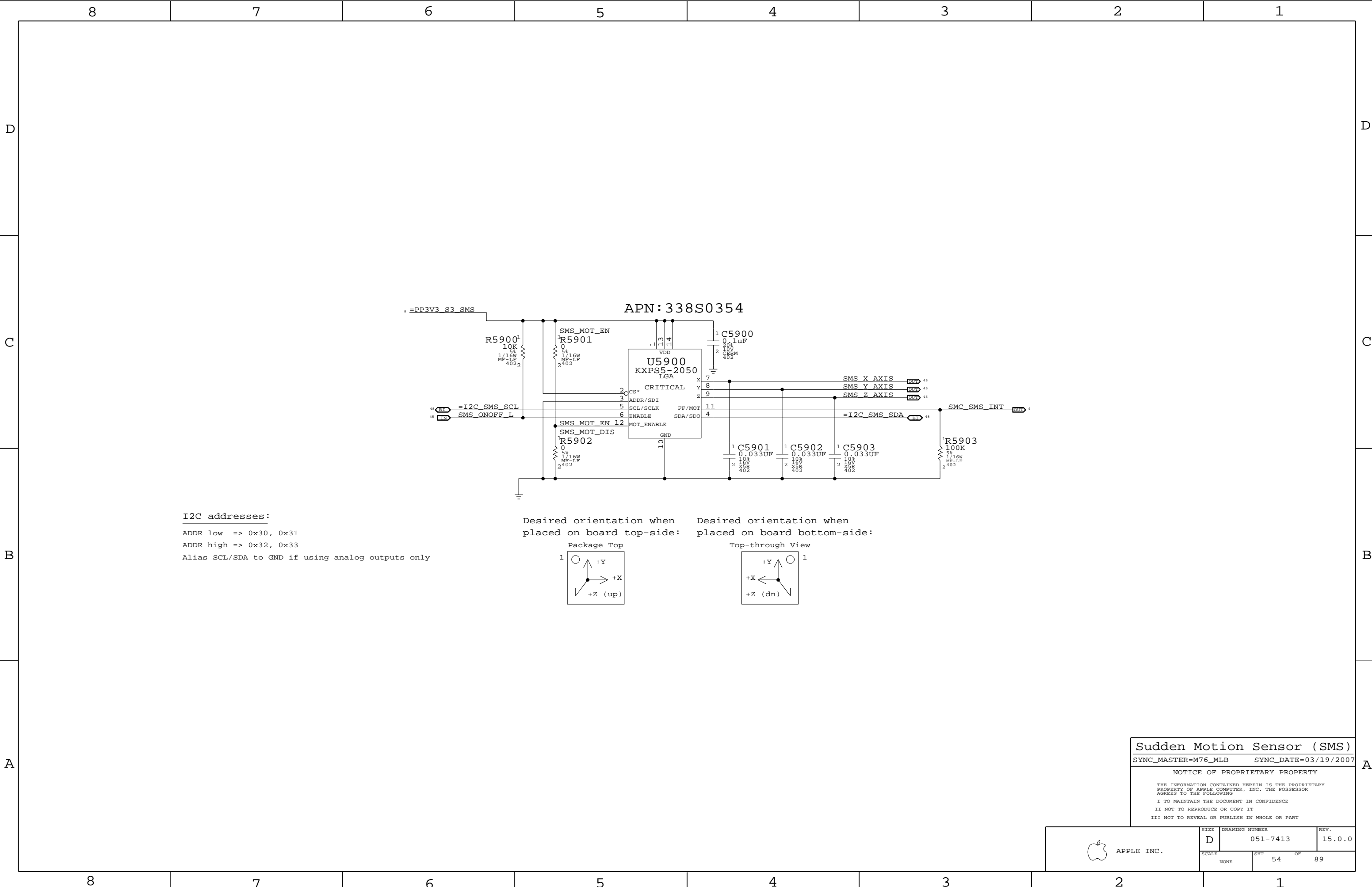
EV.	
15.0.0	

SCALE	NON
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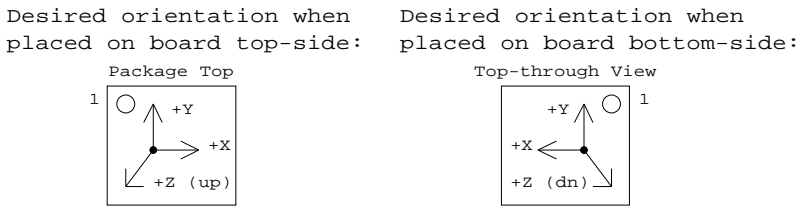
SHT

52

32



I2C addresses:
ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only



Sudden Motion Sensor (SMS)
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

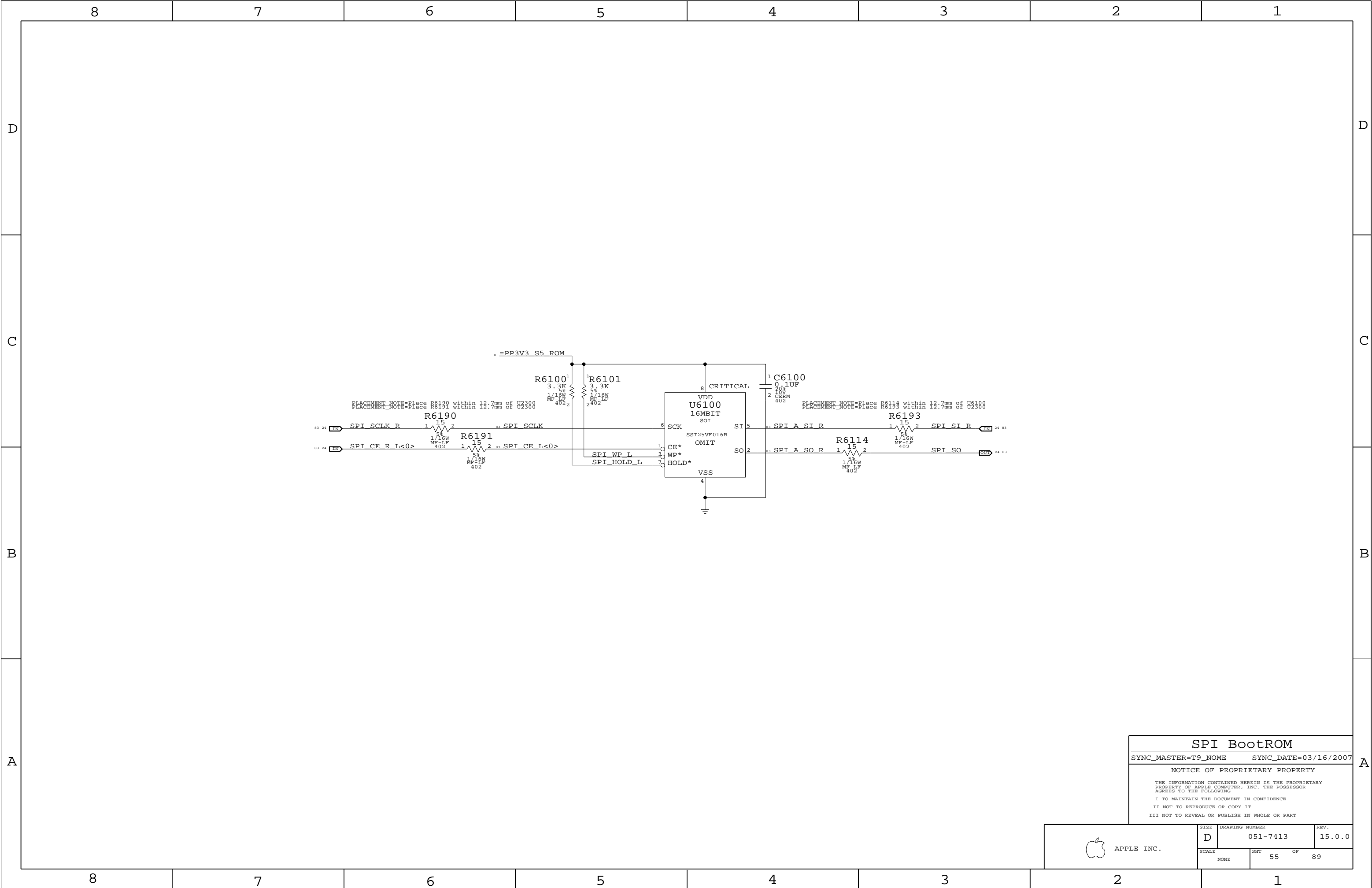
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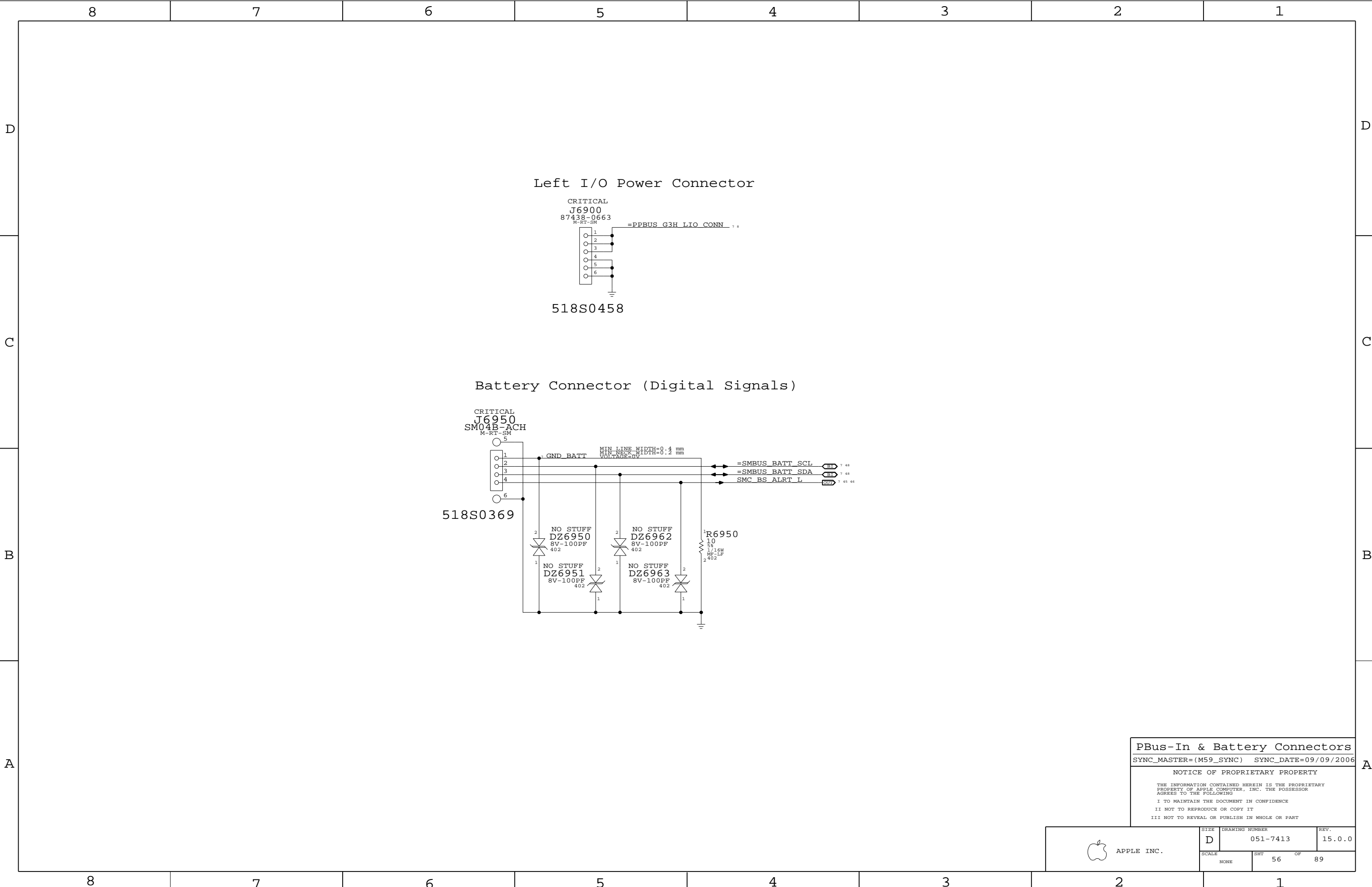
APPLE INC.	SIZE D	DRAWING NUMBER 051-7413	REV. 15.0.0
	SCALE NONE	SHT 54	OF 89



SPI BootROM		
SYNC_MASTER=T9_NOME		SYNC_DATE=03/16/2007
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SIZE D	DRAWING NUMBER 051-7413	REV. 15.0.0
	SCALE NONE	SHT 55 OF 89



APPLE INC.



PBus-In & Battery Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=09/09/2006

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7413

REV.

15.0.0

SCALE

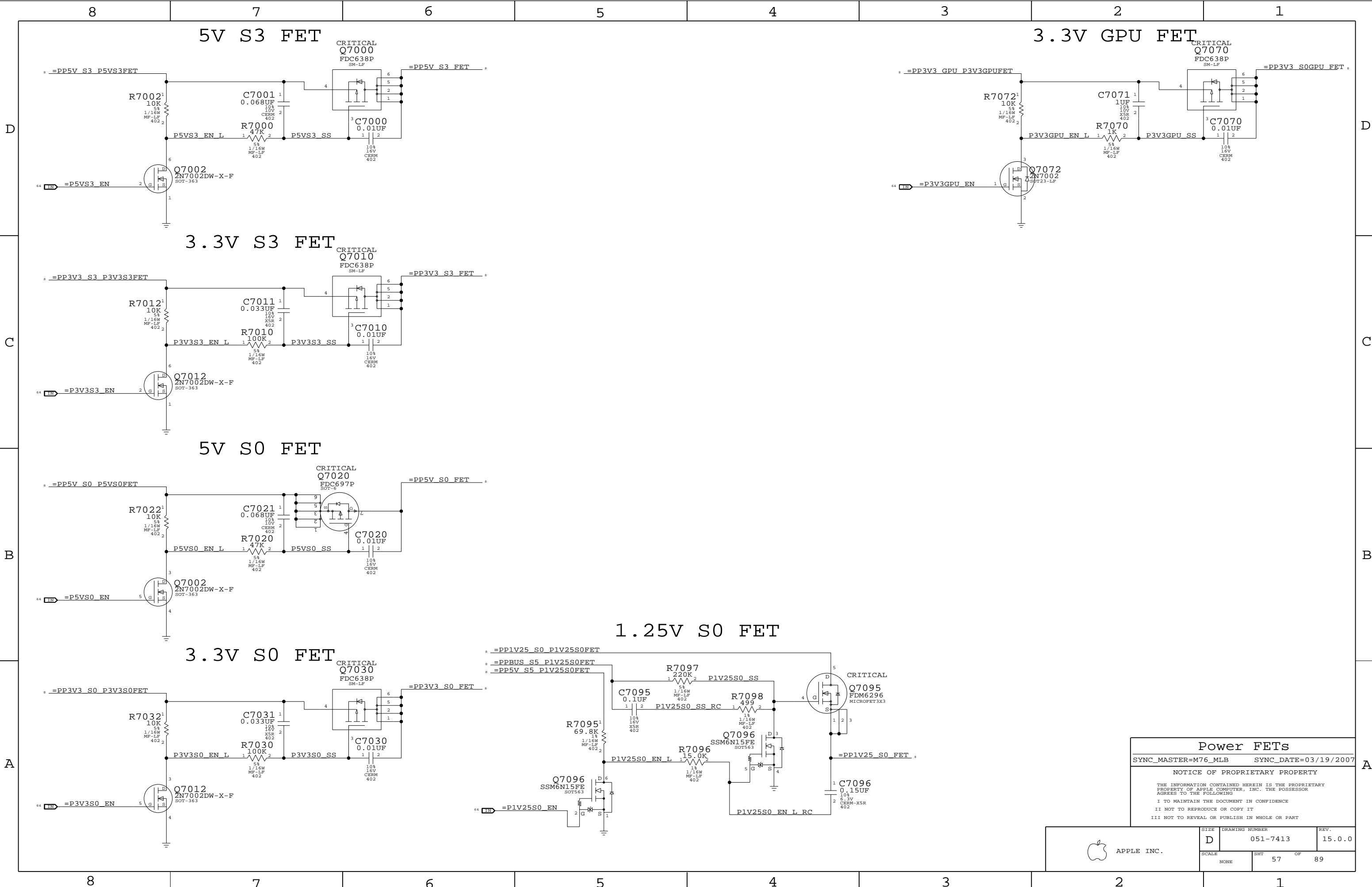
NONE

SHT

56

OF

89



Power FETs

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

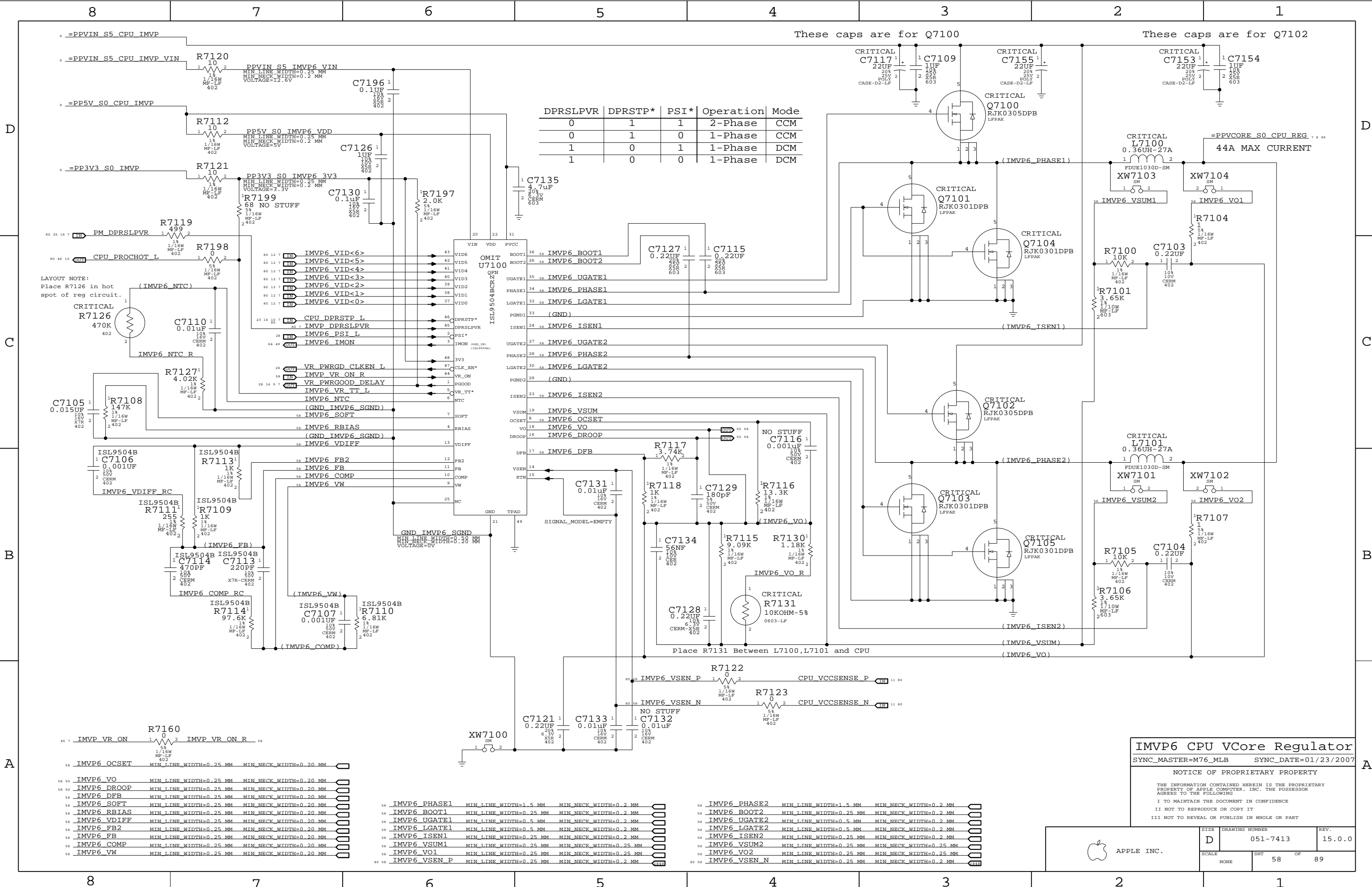
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	D	051-7413	15.0.0
SCALE		SHT	OF
NONE		57	89



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

IMVP6 CPU VCore Regulator
SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

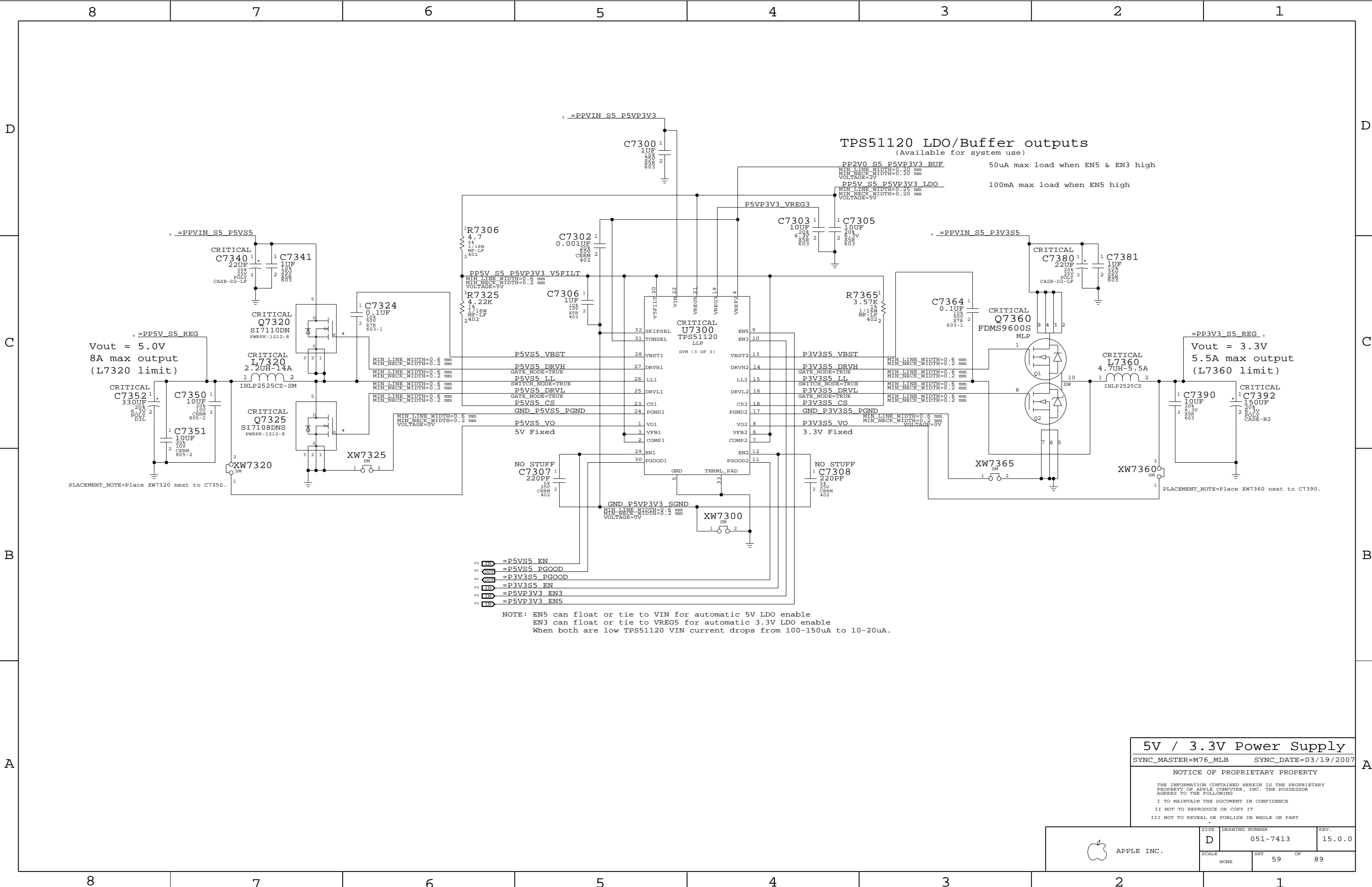
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	58	89



5V / 3.3V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

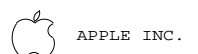
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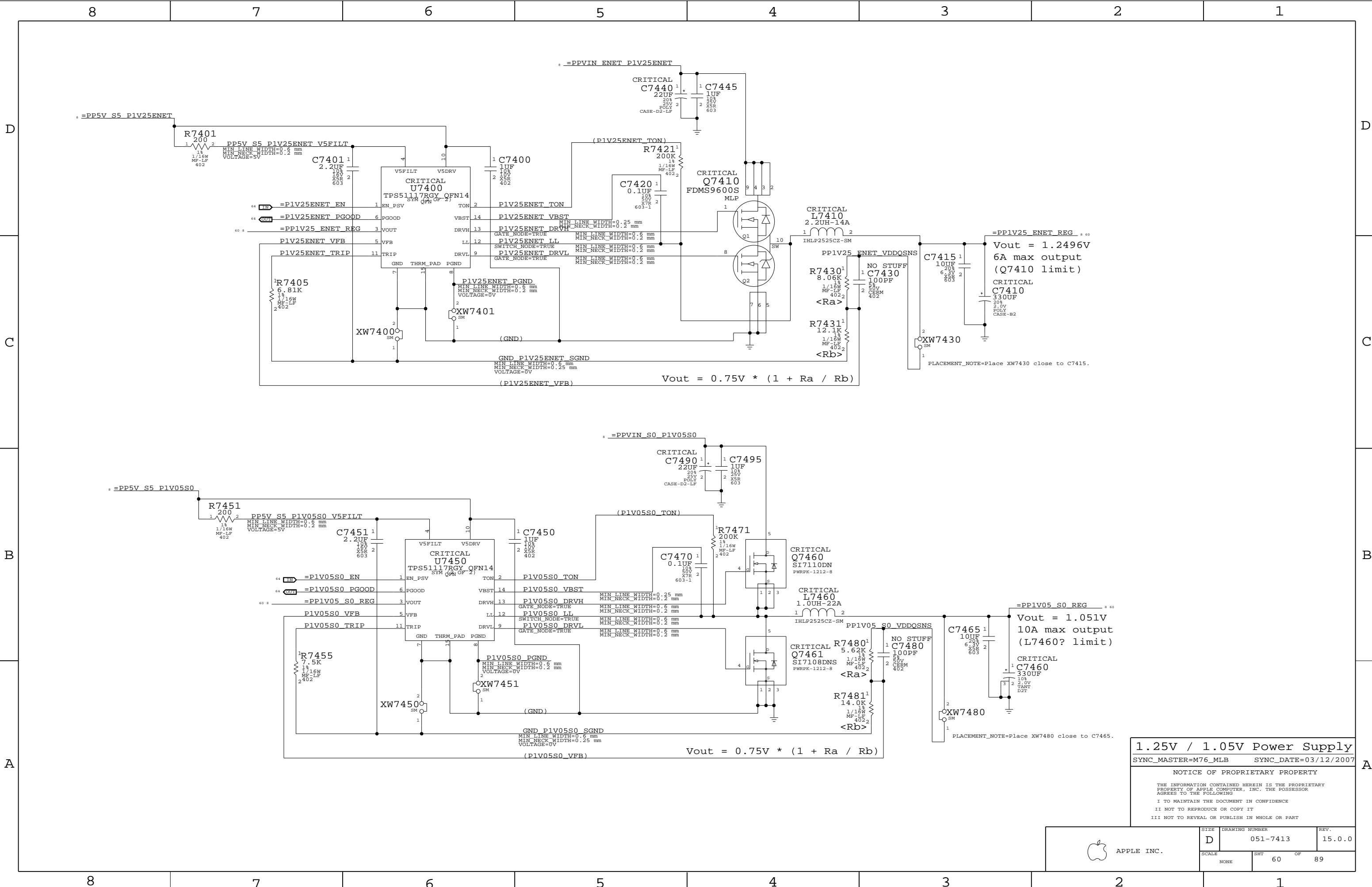
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	59	89



1.25V / 1.05V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

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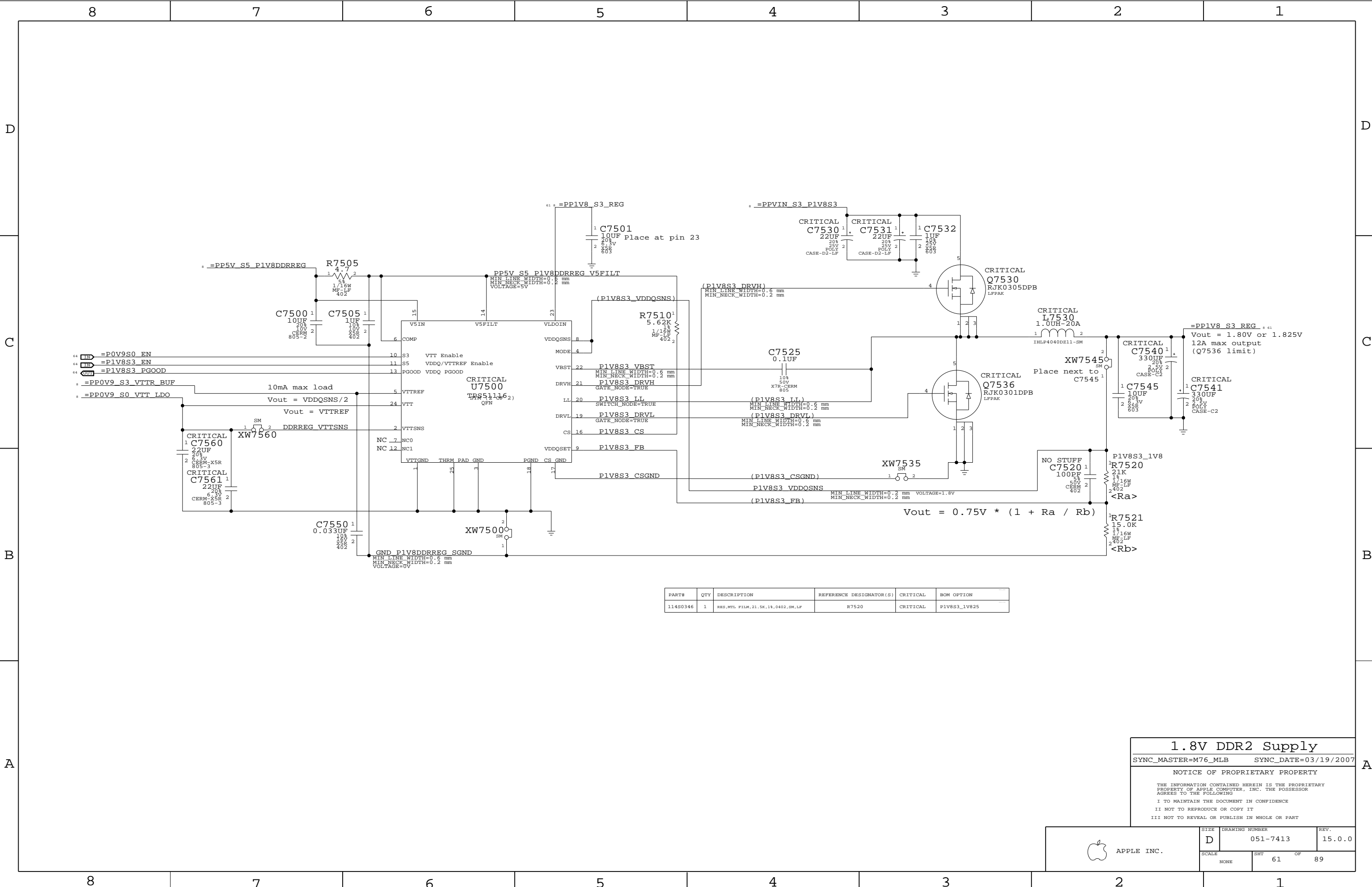
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	60	89



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0346	1	RES,MTL FILM,21.5K,1%,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V825

1.8V DDR2 Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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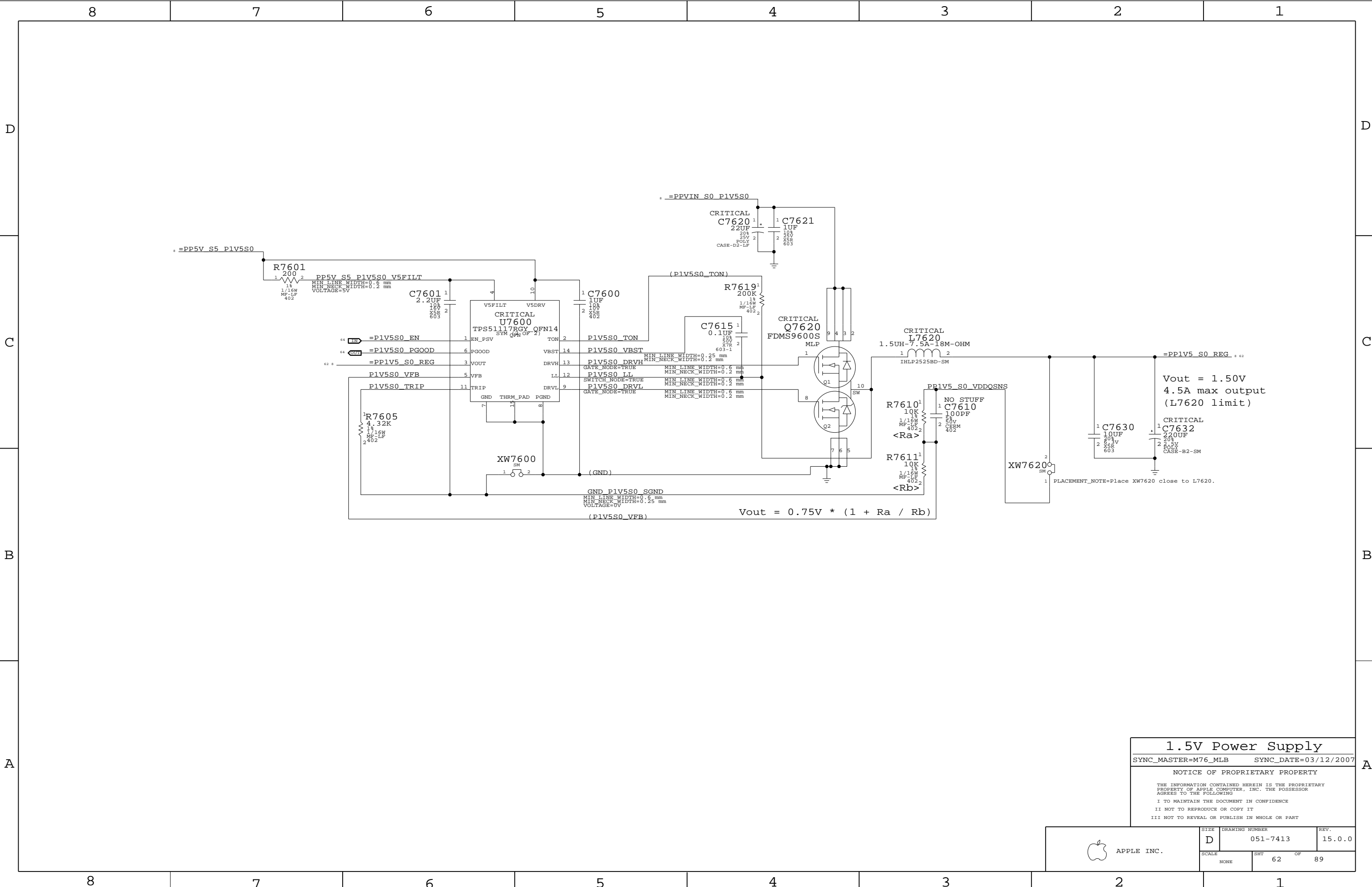
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APPLE INC.

SIZE D	DRAWING NUMBER 051-7413	REV. 15.0.0
SCALE NONE	SHT 61	OF 89



1.5V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

NOTICE OF PROPRIETARY PROPERTY

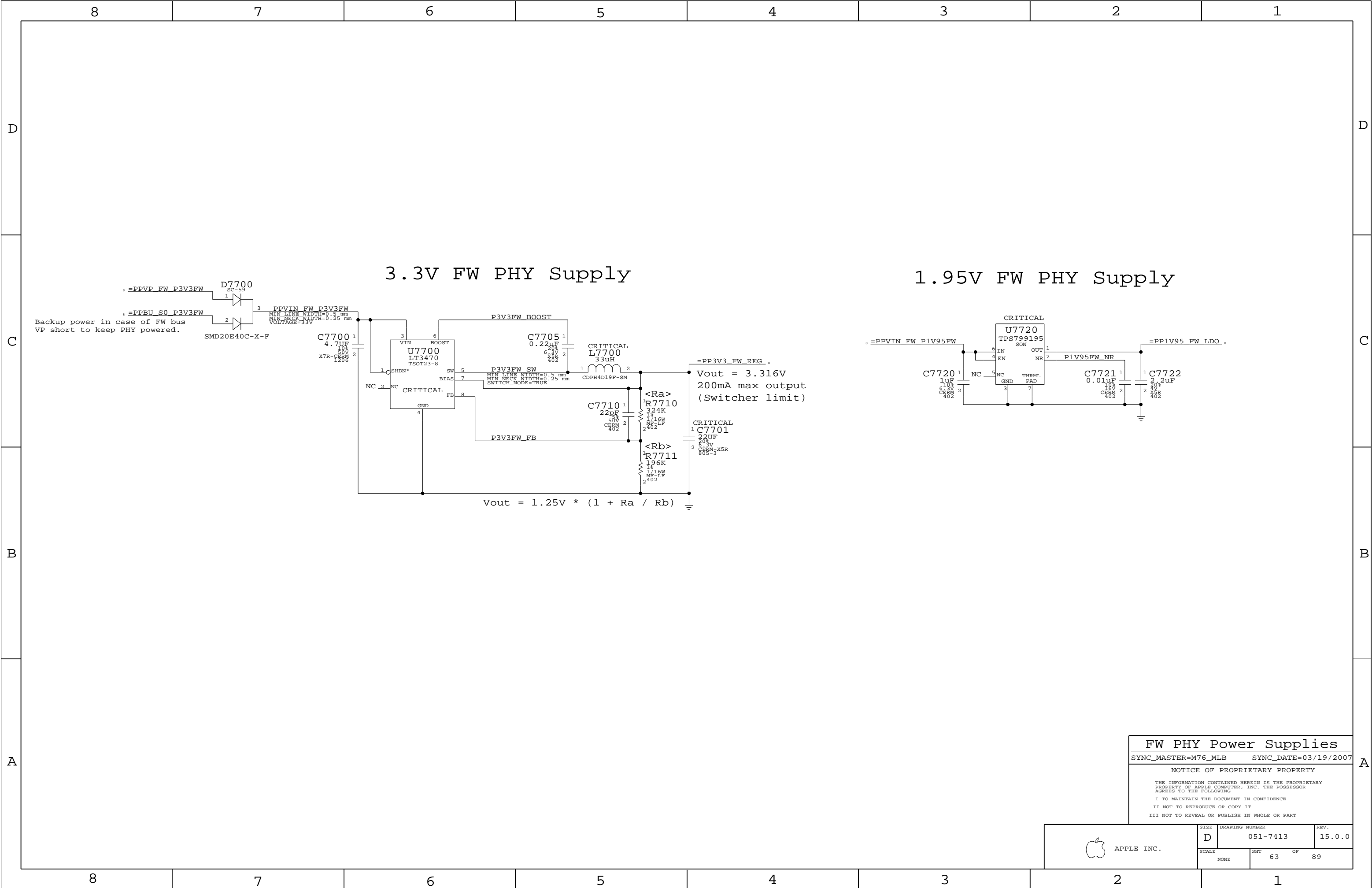
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7413	15.0.0
SCALE		SHT	OF
NONE		62	89



FW PHY Power Supplies

SYNC_MASTER=M76_MLB

SYNC_DATE=03/19/2007


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 APPLE INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7413		15.0.0
SCALE		SHT	OF	
NONE		63	89	

Power Control Signals

3.425V "G3Hot" Supply

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

Supply needs to guarantee 3.31V delivered to SMC Vref generator

Vout = 3.425
200mA max output
(Switcher limit)

$$V_{out} = 1.25V * (1 + R_a / R_b)$$

Unused PGOOD Signals

- =P1V25ENET PGOOD == TP P1V25ENET PGOOD
- =P1V8_S0GPU PGOOD == TP P1V8_S0GPU PGOOD

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

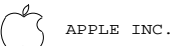
NOTE: 0.9V is not checked!
Other S0 Rails PWRGD Circuit

3.425V G3Hot Supply & Power Control

SYNC_MASTER=M88 SYNC_DATE=08/02/2007

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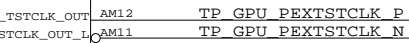
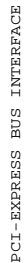
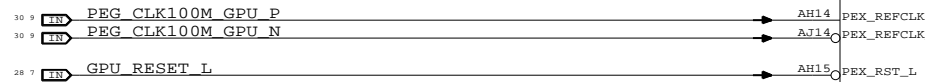
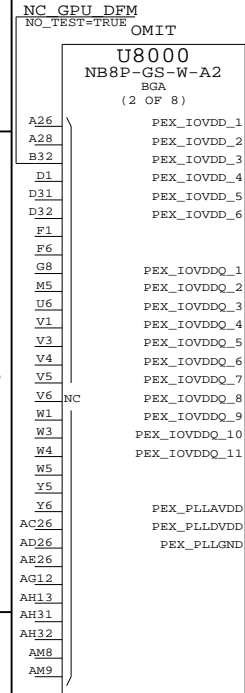
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	64	89


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Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD
```

```
Signal aliases required by this page:
(NONE)
```

```
BOM options provided by this page:
(NONE)
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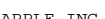


SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER
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051-7413

15.0.0

SHT 65

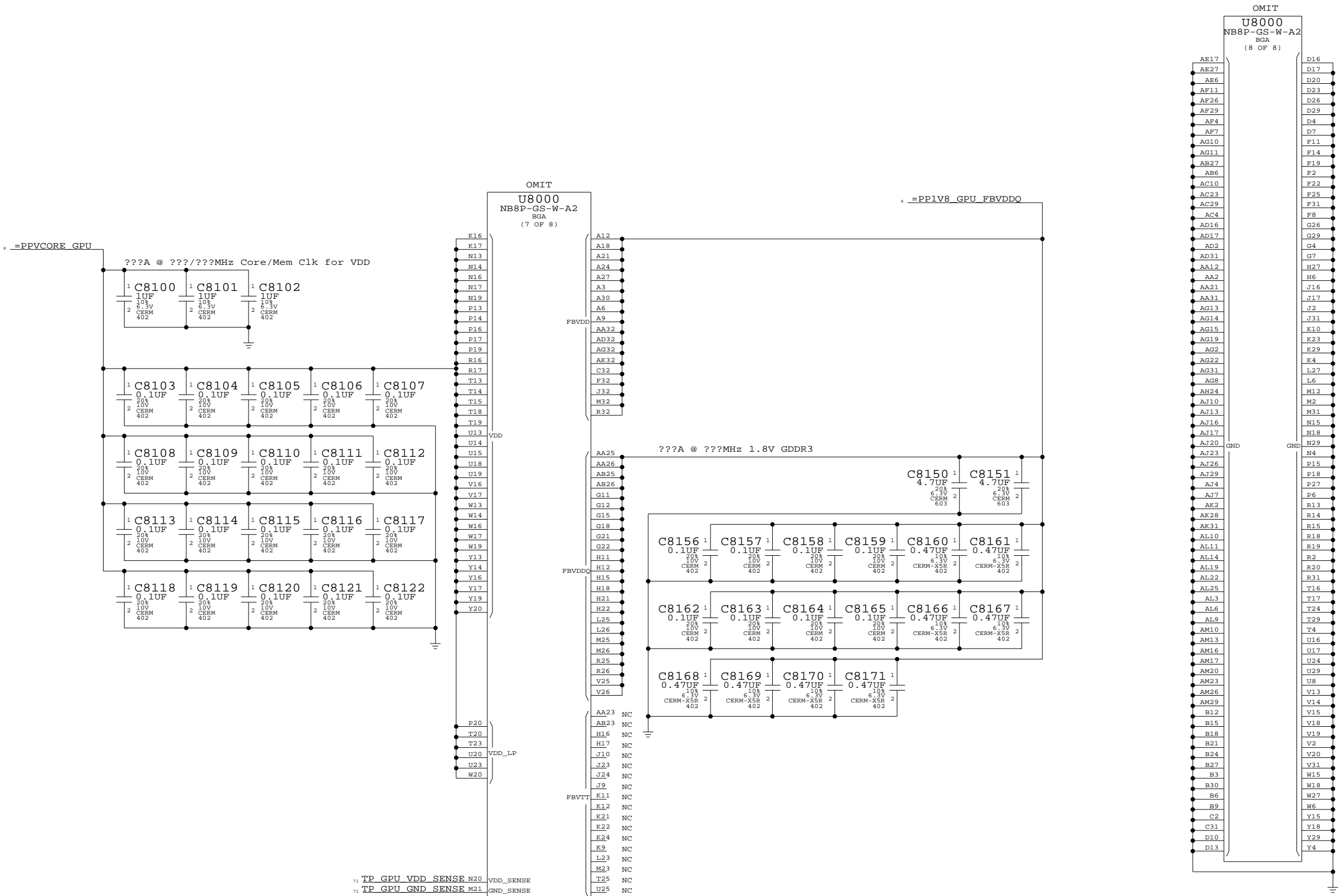
SHT 65

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Core/FB Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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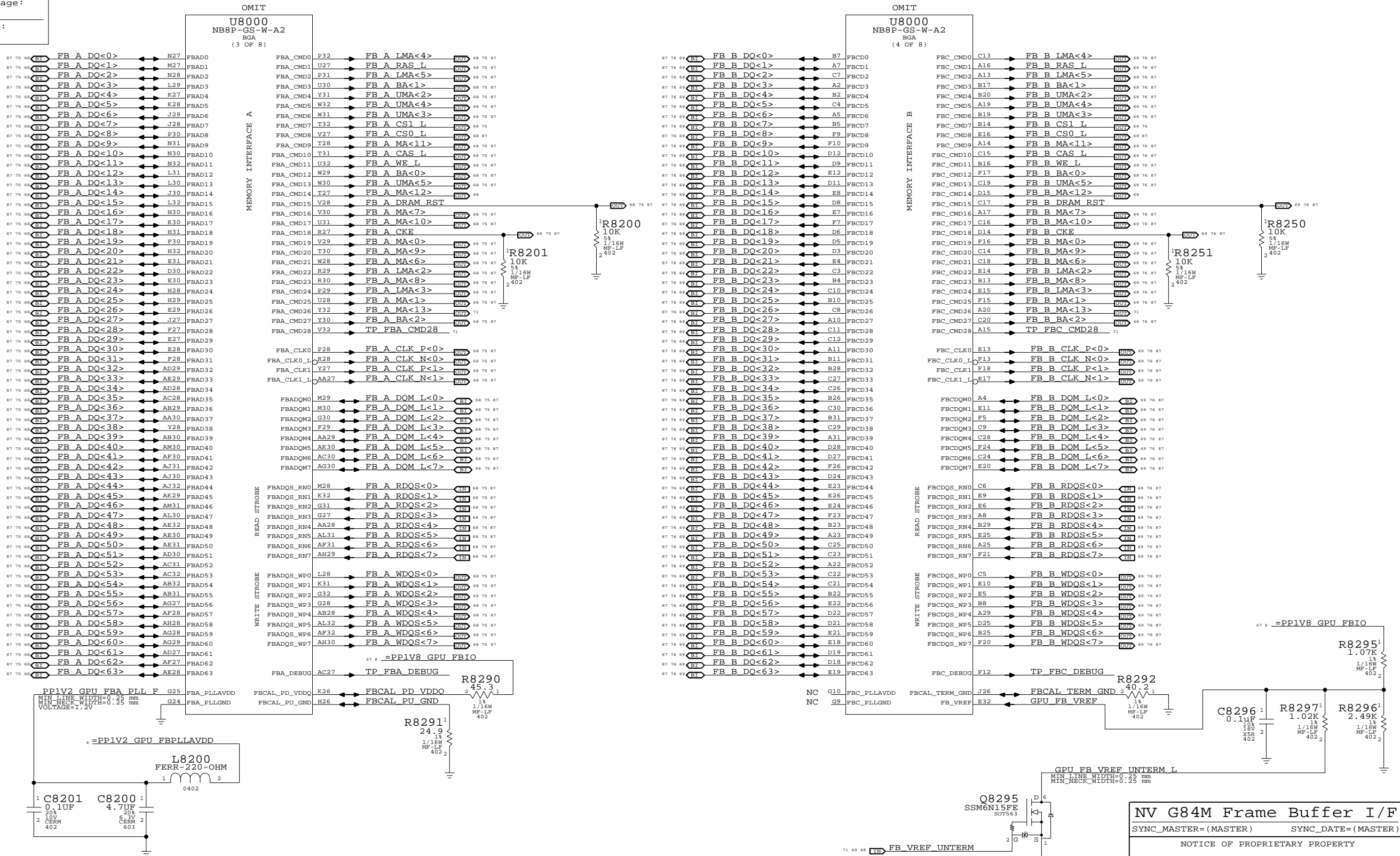
SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	66	89

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

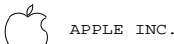
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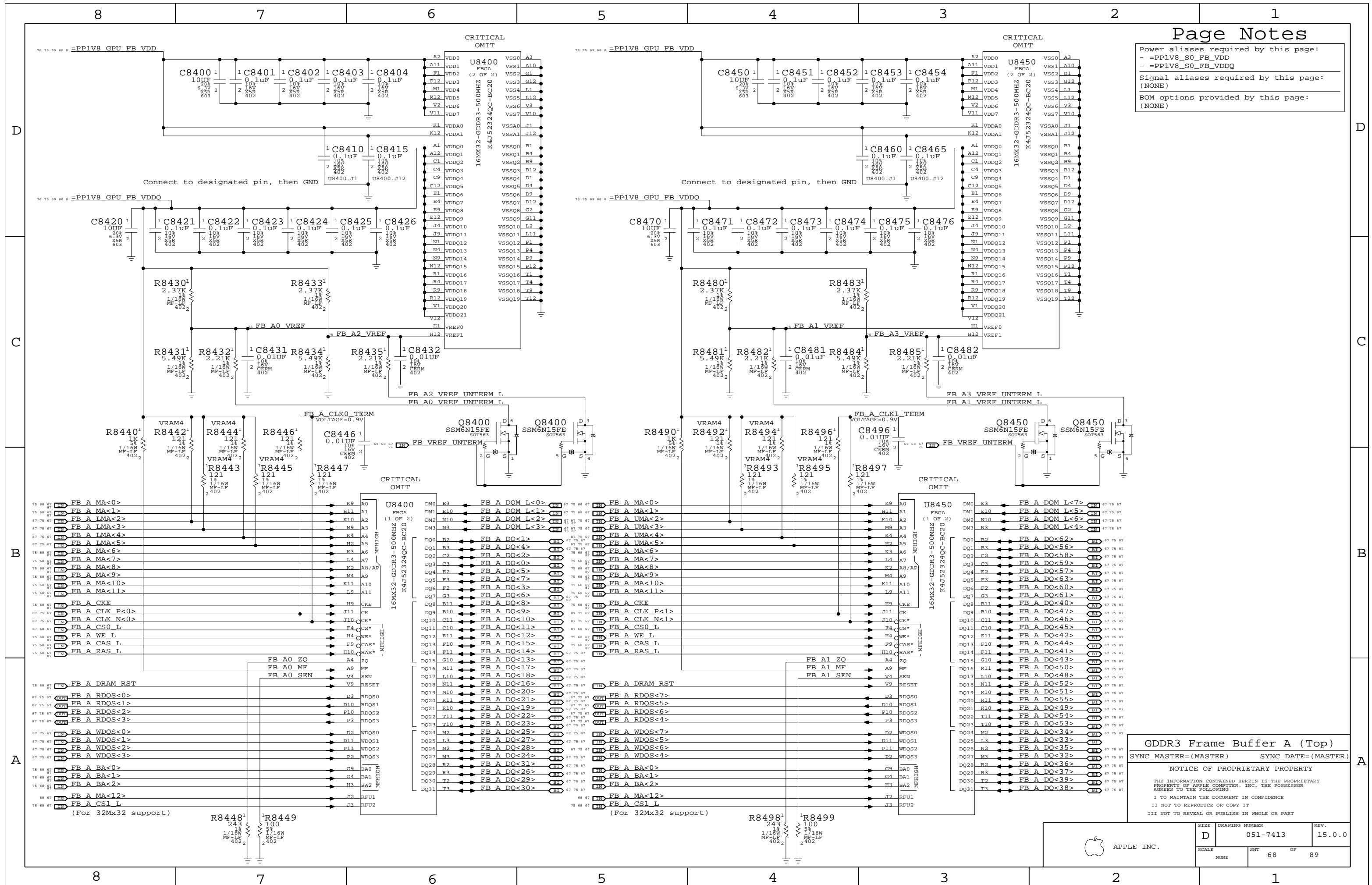
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

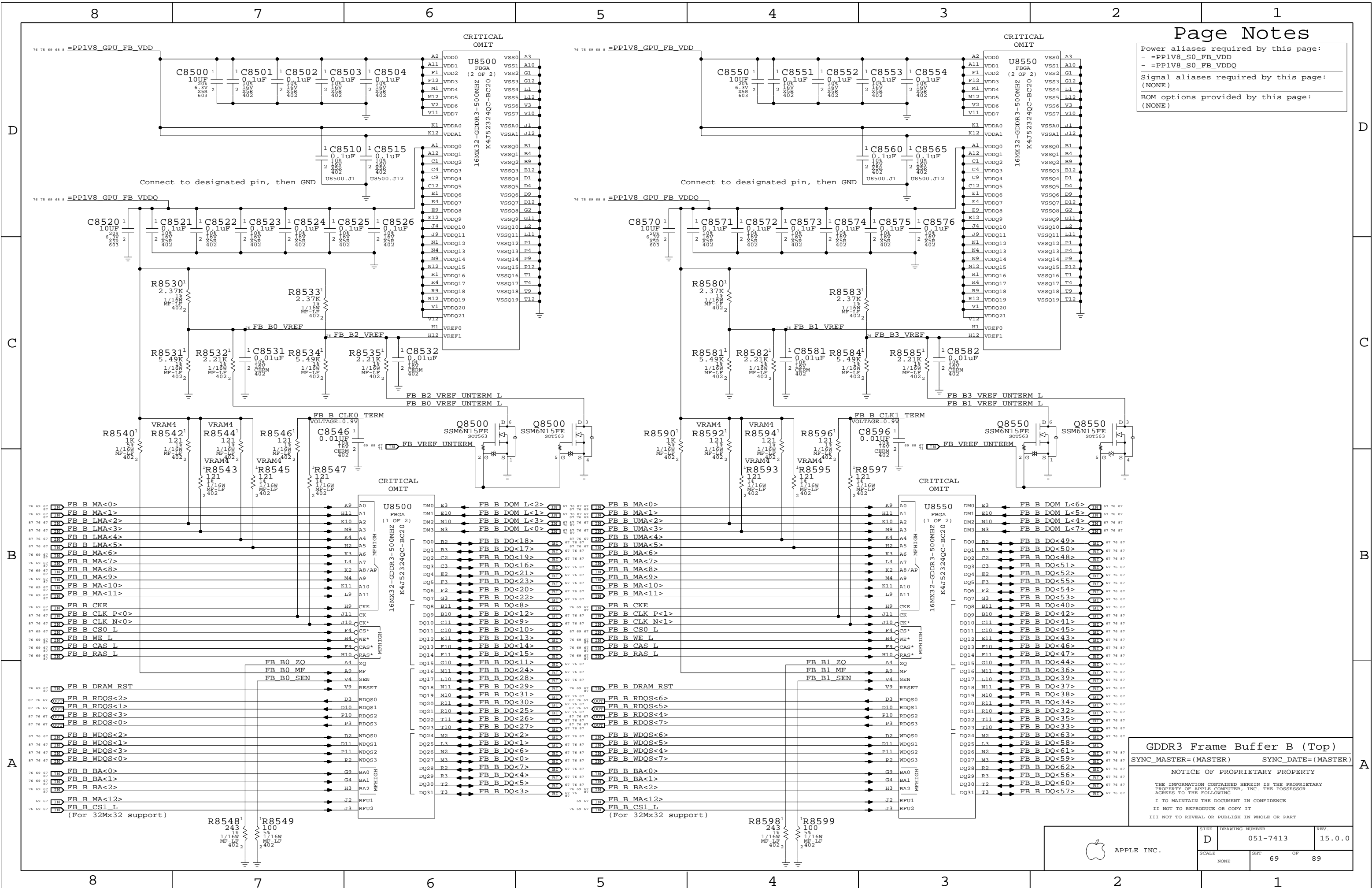
SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	67	89



Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B (Top)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

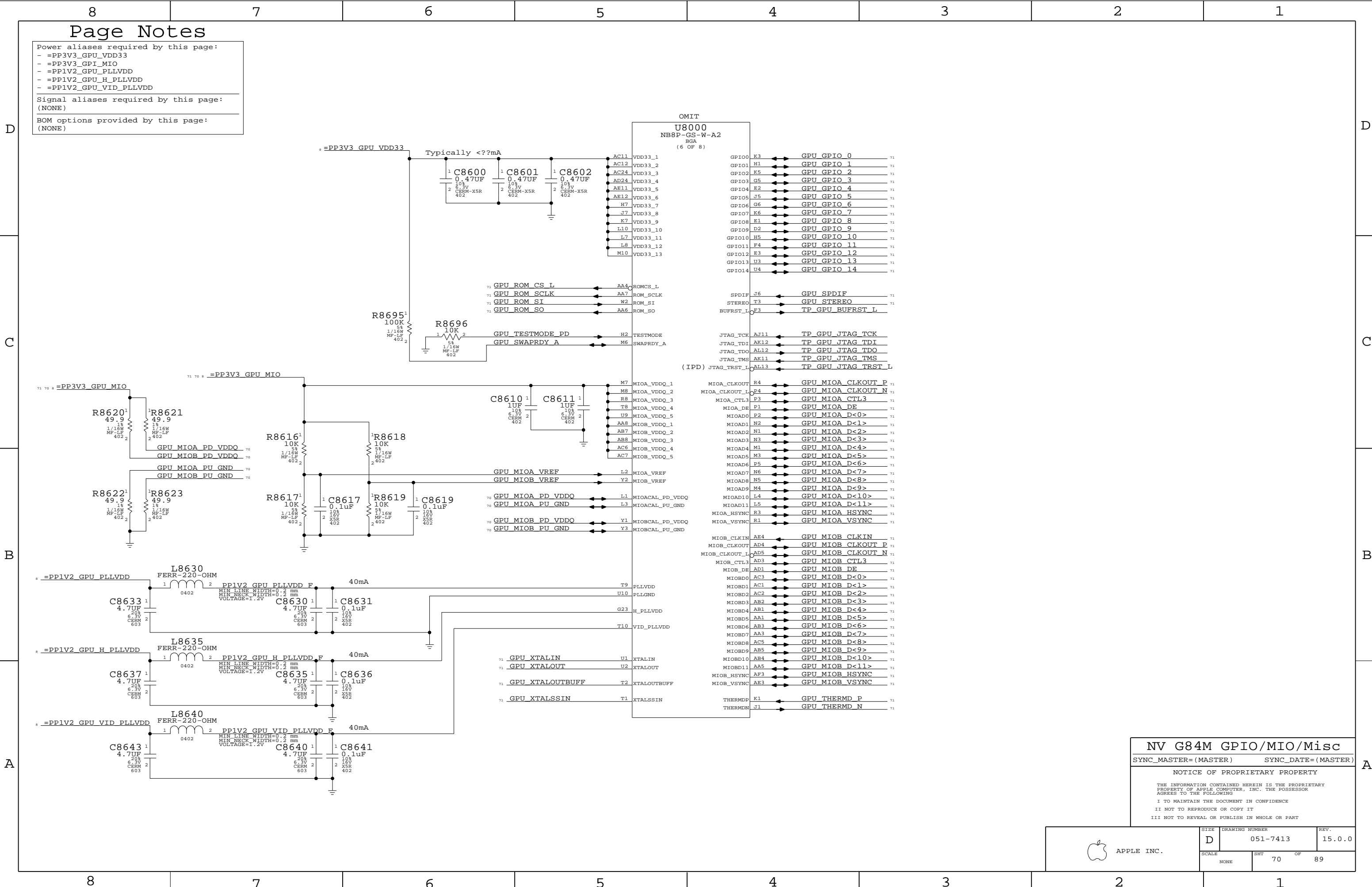
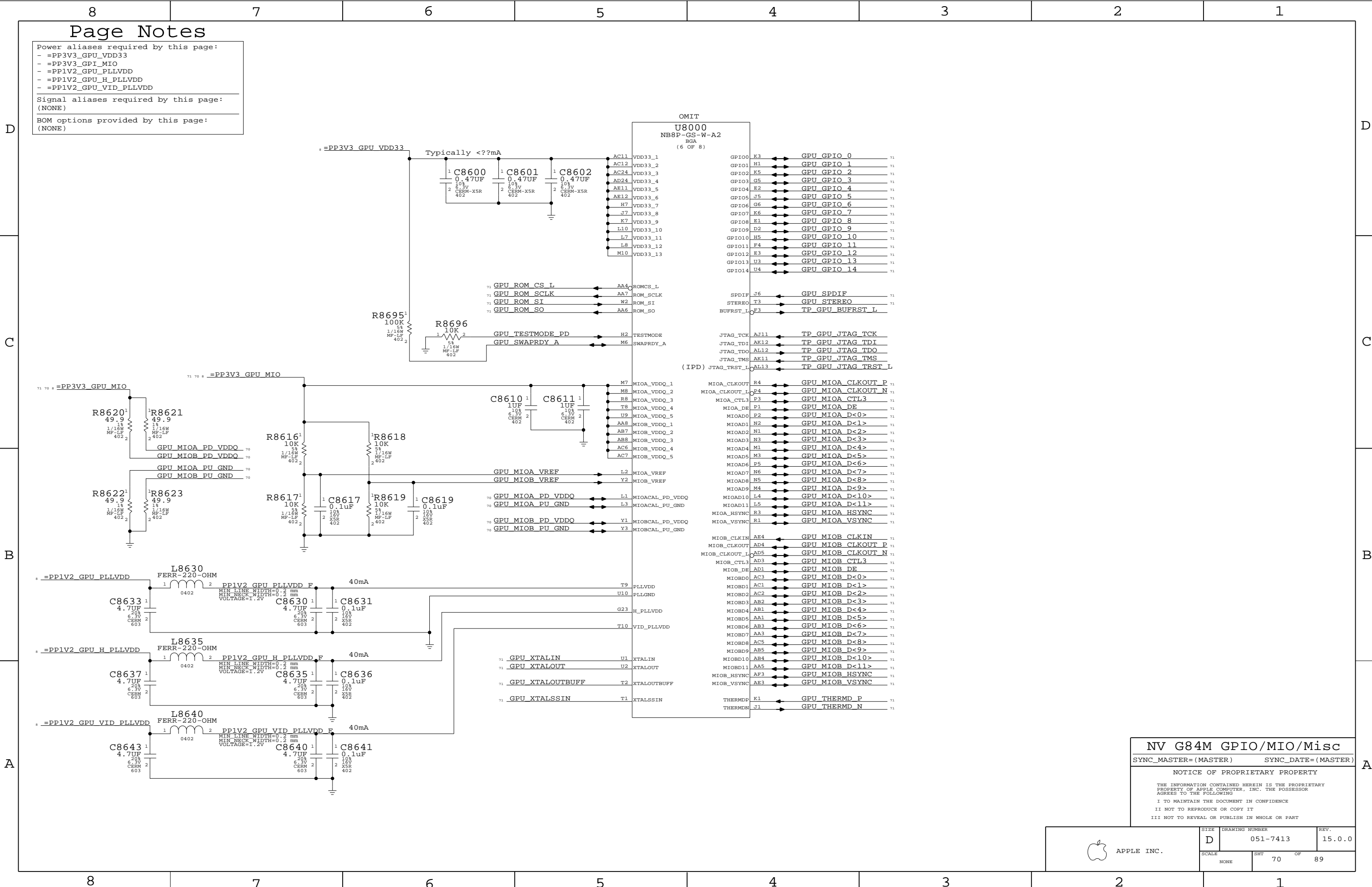
NOTICE OF PROPRIETARY PROPERTY

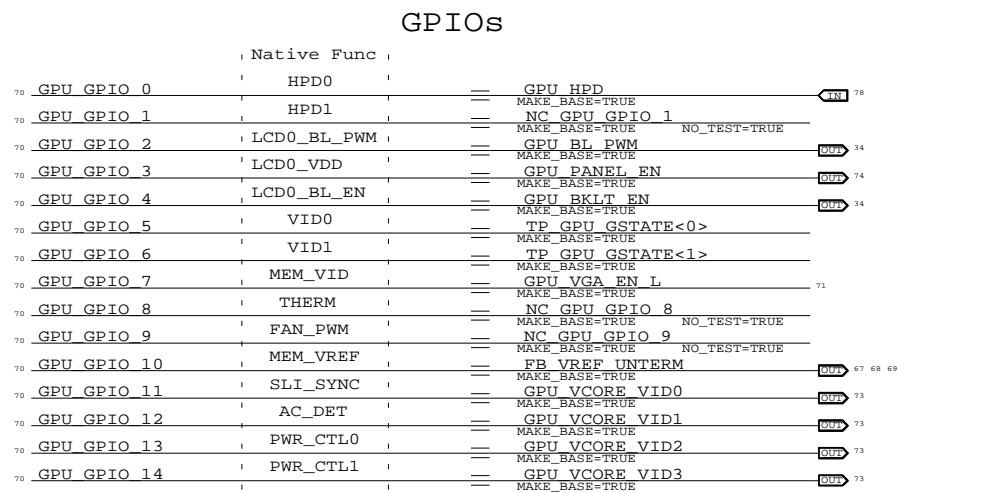
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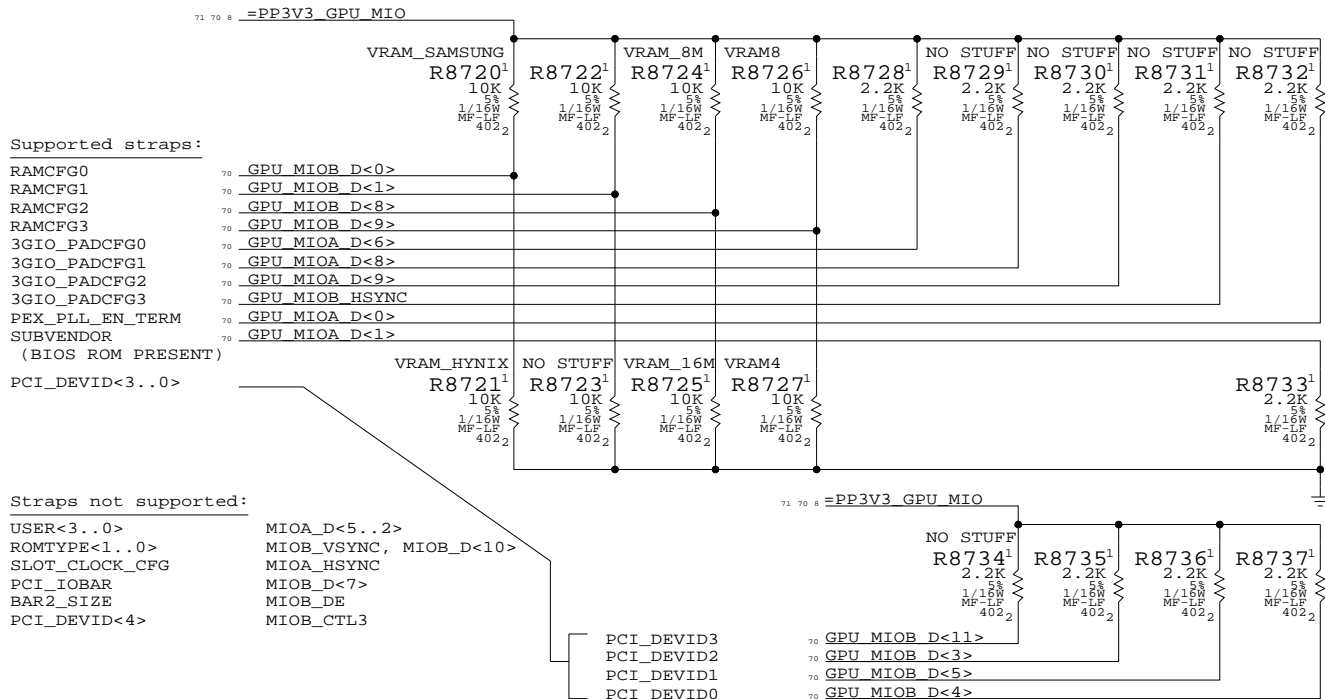


SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	69	89

[illegible][illegible][illegible][illegible][illegible][illegible][illegible][illegible]



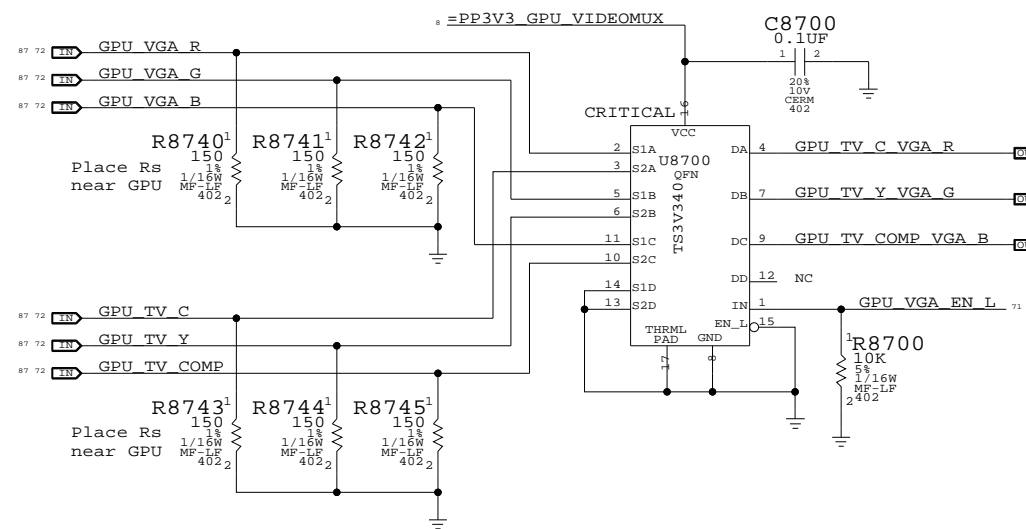
Config Straps



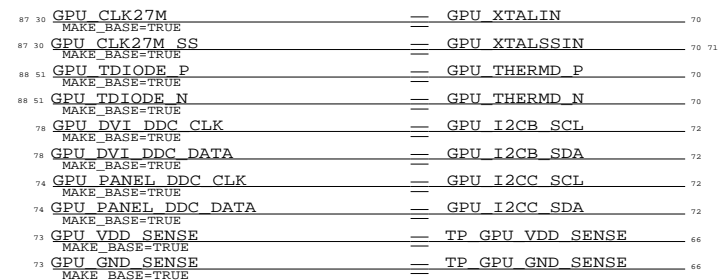
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└─ pci_device % ─┘
Analog Video Mux

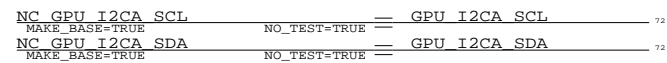
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Renamed signals

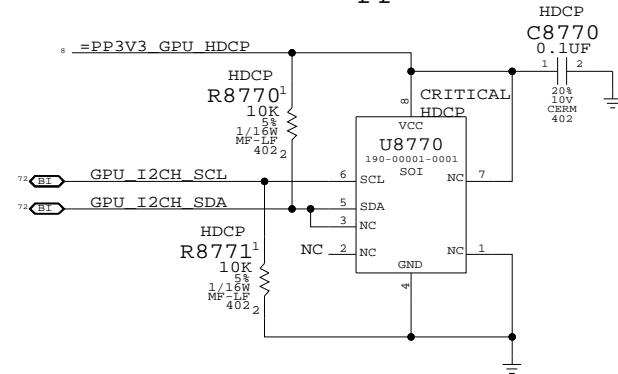


Unused I2C Buses

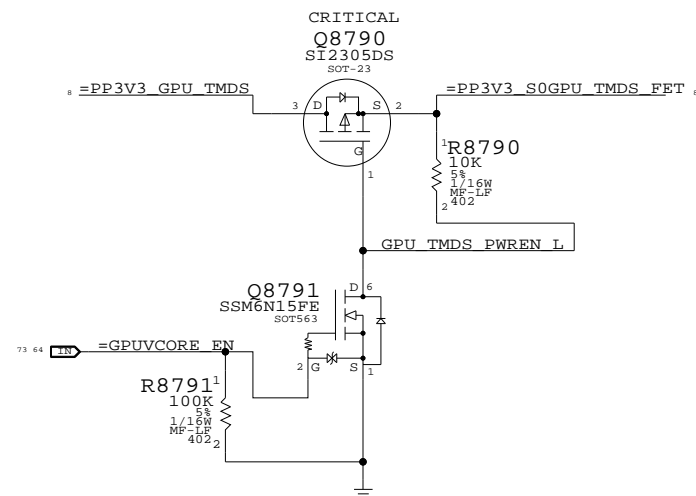


I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

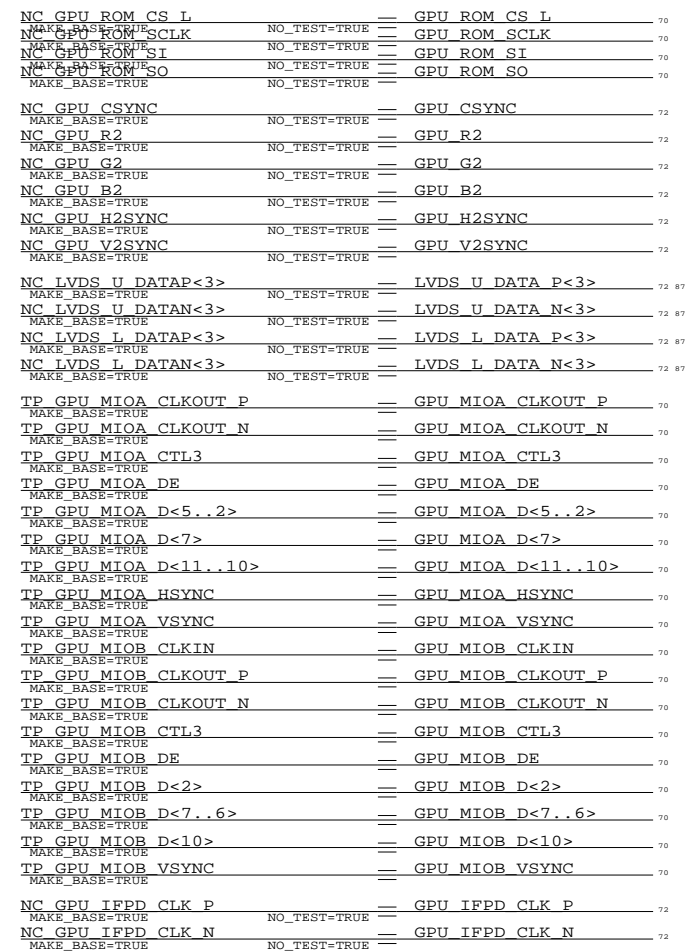
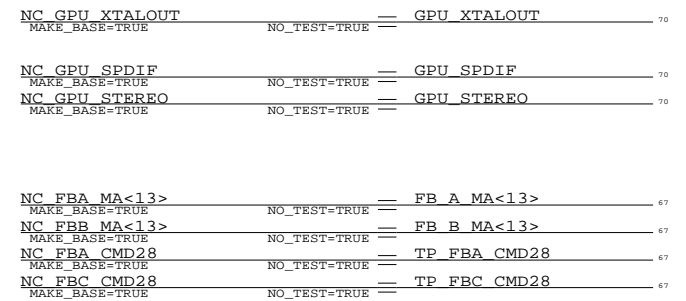
HDCP Support



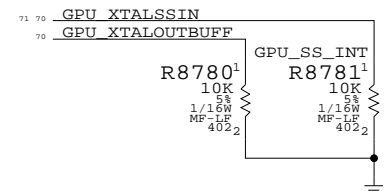
TMDS Backdrive Protection



Unused signals



Unused Clocks



GPU Straps

SYNC_MASTER=M88	SYNC_DATE=08/02/2007
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	SIZE
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DRAWING NUMBER

REV.	15.0.0
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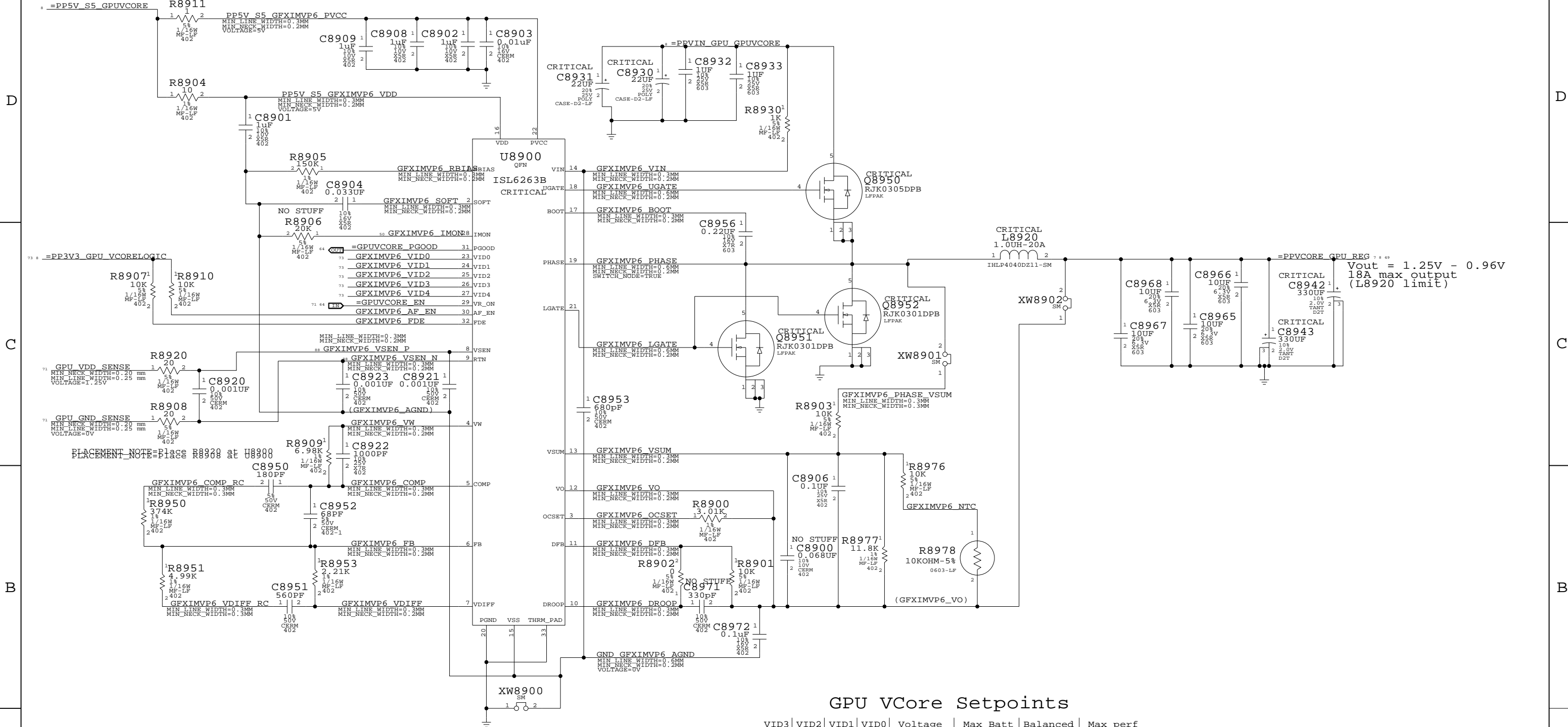
SCALE

	SHT
--	-----

SHT 71

22

GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	0	1	1.05575V	M87,M88	M87	-
0	1	1	0	1.13300V	-	M88	M87
0	0	1	0	1.23600V	-	-	M88

Other VID states may not be valid

M87/M88 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P26V	GPUVID3_0,GPUVID2_0,GPUVID1_1,GPUVID0_0
GPUVID_1P13V	GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_0
GPUVID_1P05V	GPUVID3_1,GPUVID2_0,GPUVID1_0,GPUVID0_1

GPU (G84M) Core Supply

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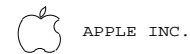
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SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	73	89

[illegible]

518S0289

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	D	051-7413	15.0.0
	SCALE	SMT OF	
	NONE	74	89

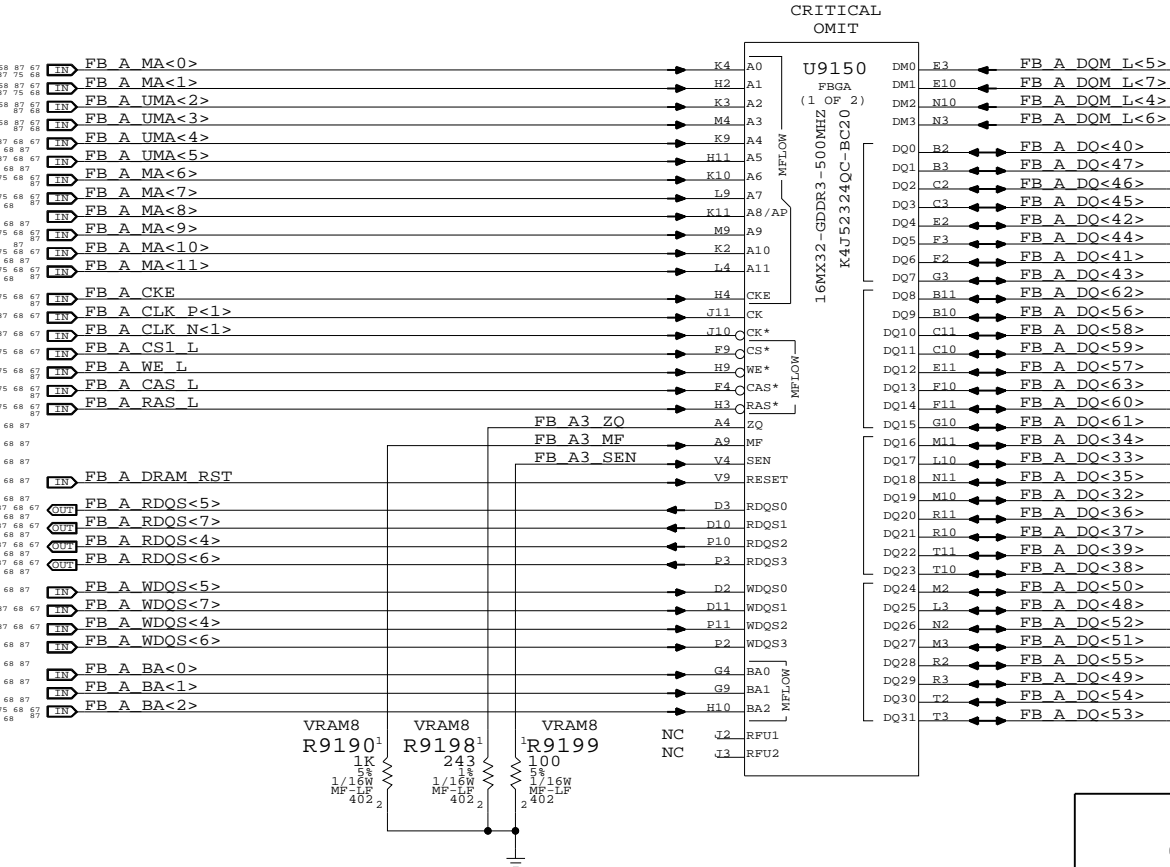
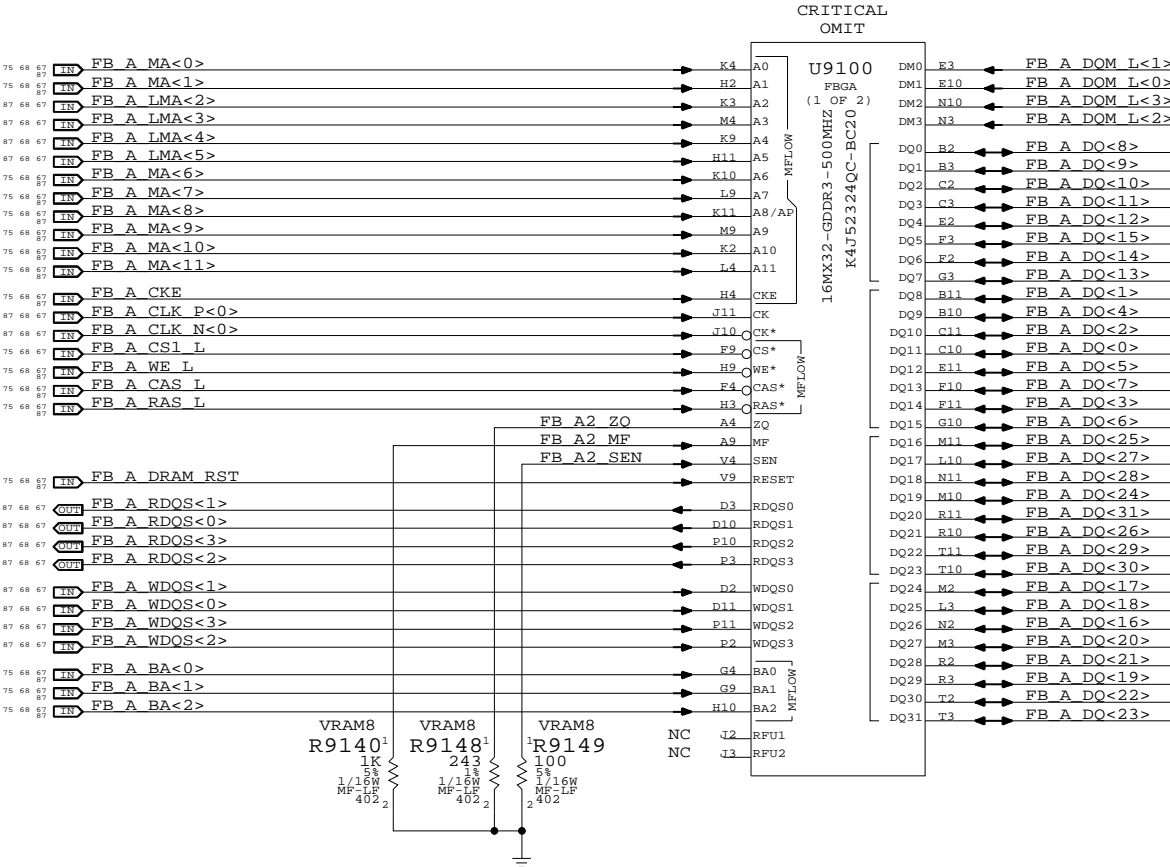
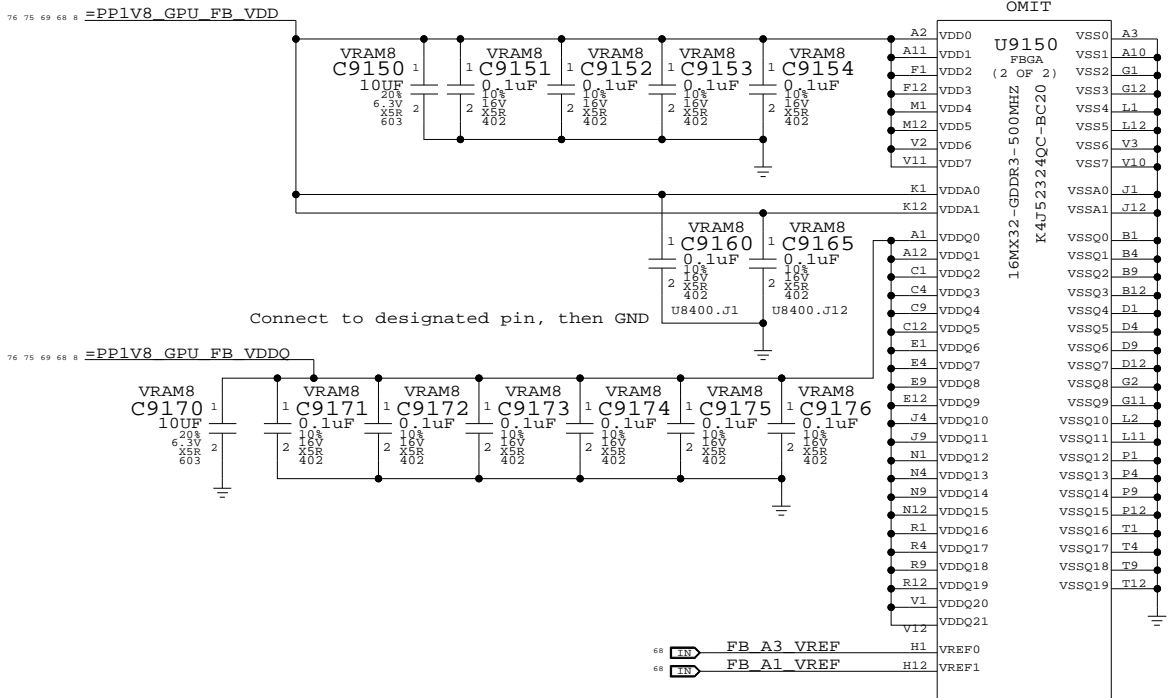
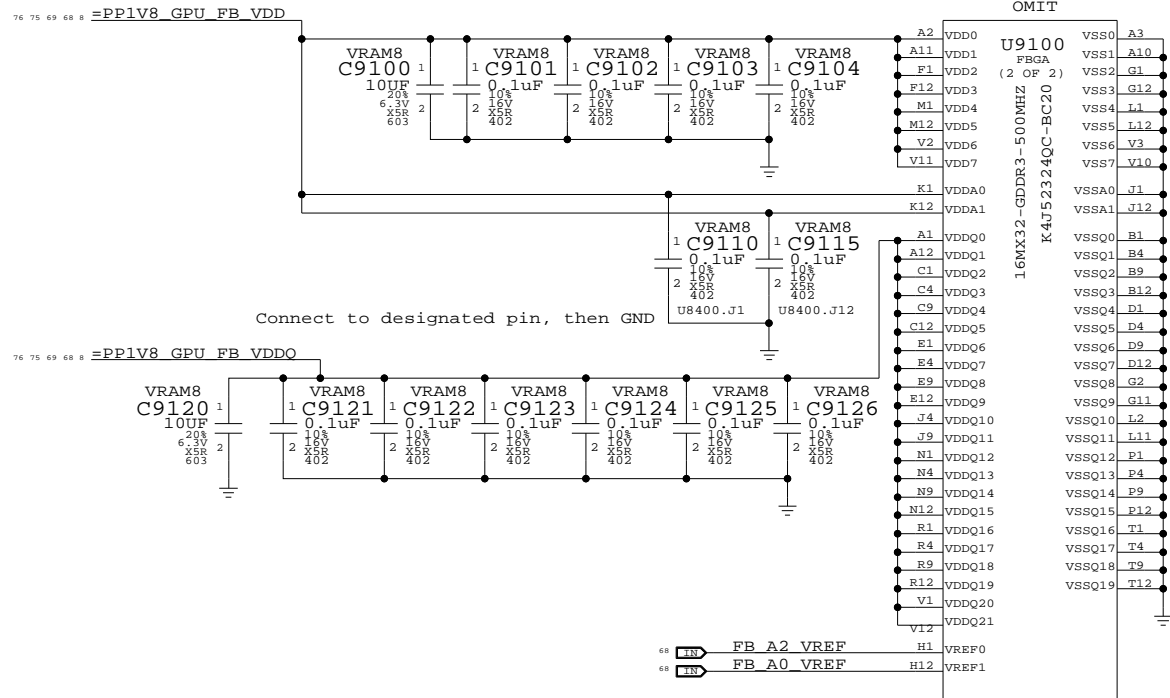


Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A (Bot)

SYNC_MASTER=M88_MLB_VRAMSNOT_DATE=06/19/2007

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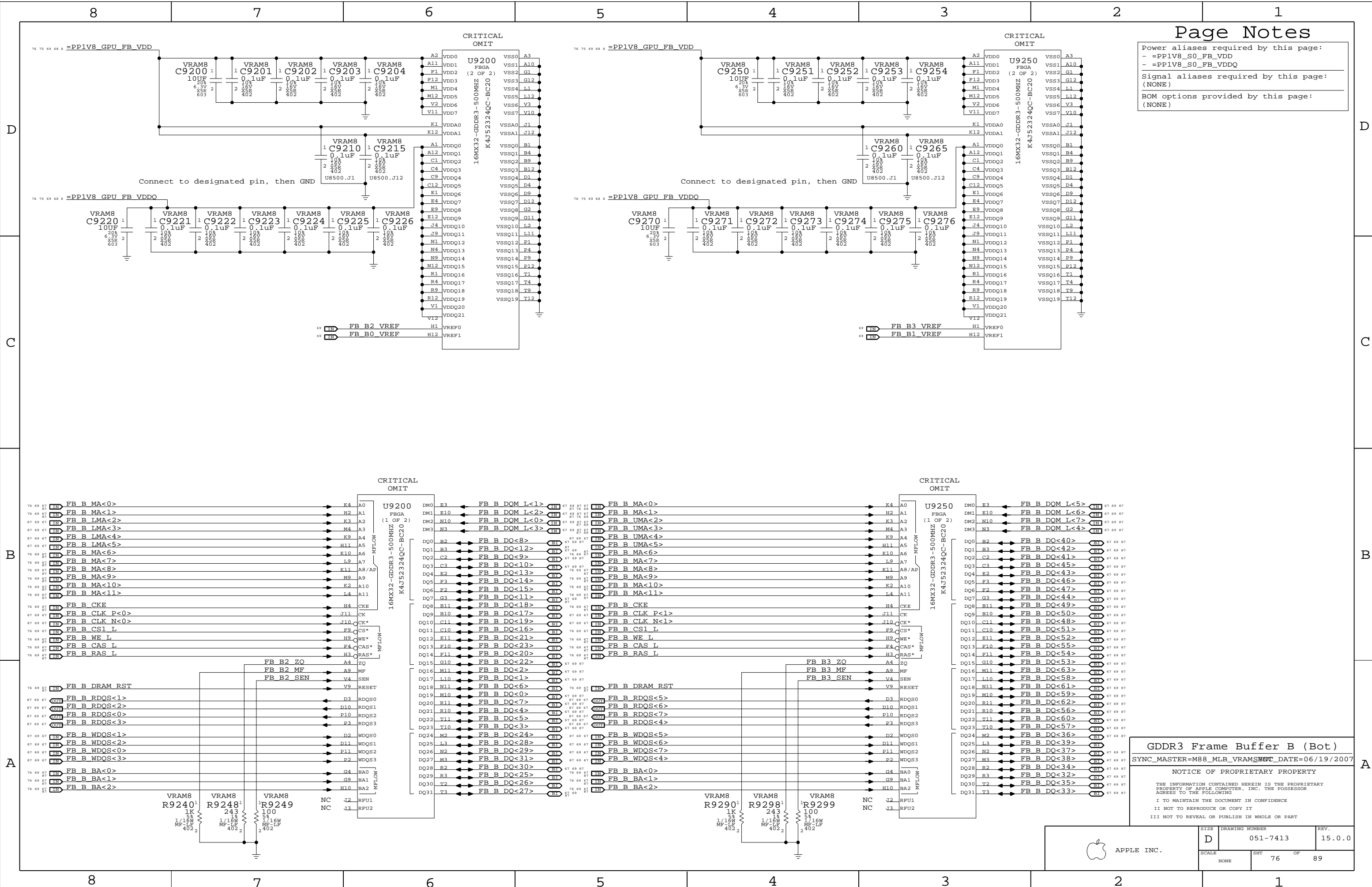
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SCALE	NONE	SHT	75	OF	89

Page Notes

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- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B (Bot)

SYNC_MASTER=M88_MLB_VRAMSNOT_DATE=06/19/2007

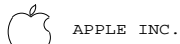
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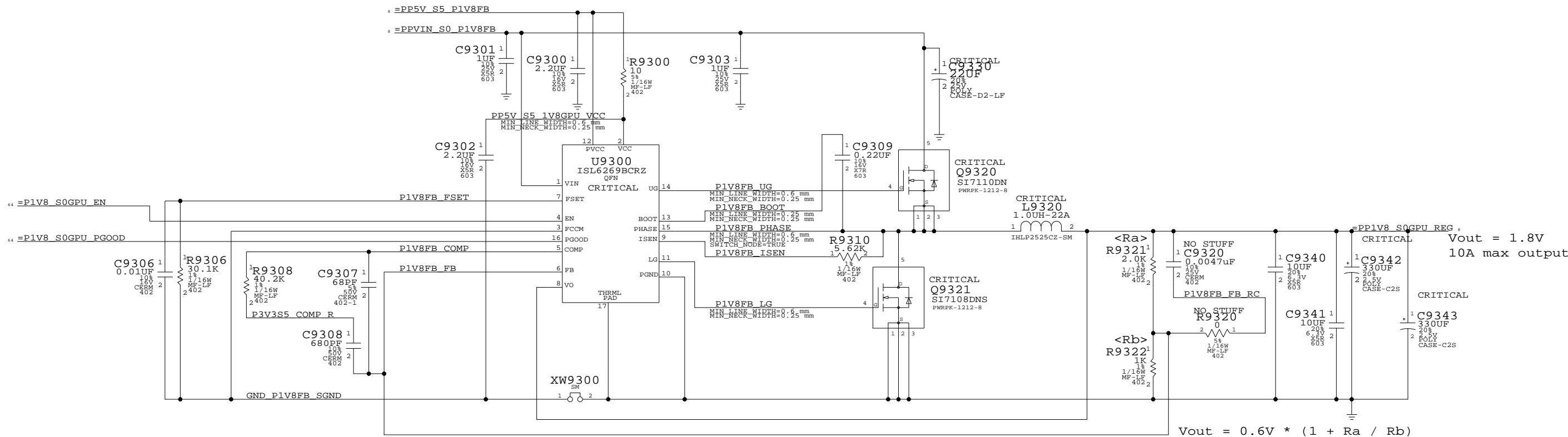
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SIZE	D	DRAWING NUMBER	051-7413	REV.	15.0.0
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1.8V Frame Buffer Regulator



1.8V FB Power Supply

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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SCALE		SHT	OF
NONE		77	89

D

C

B

A

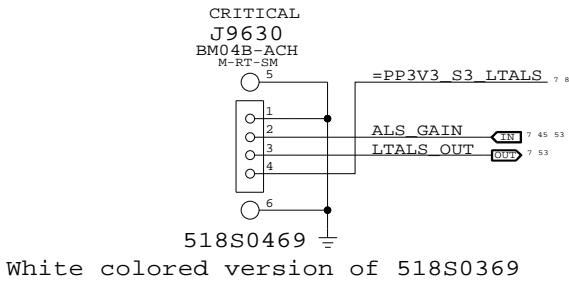
D

C

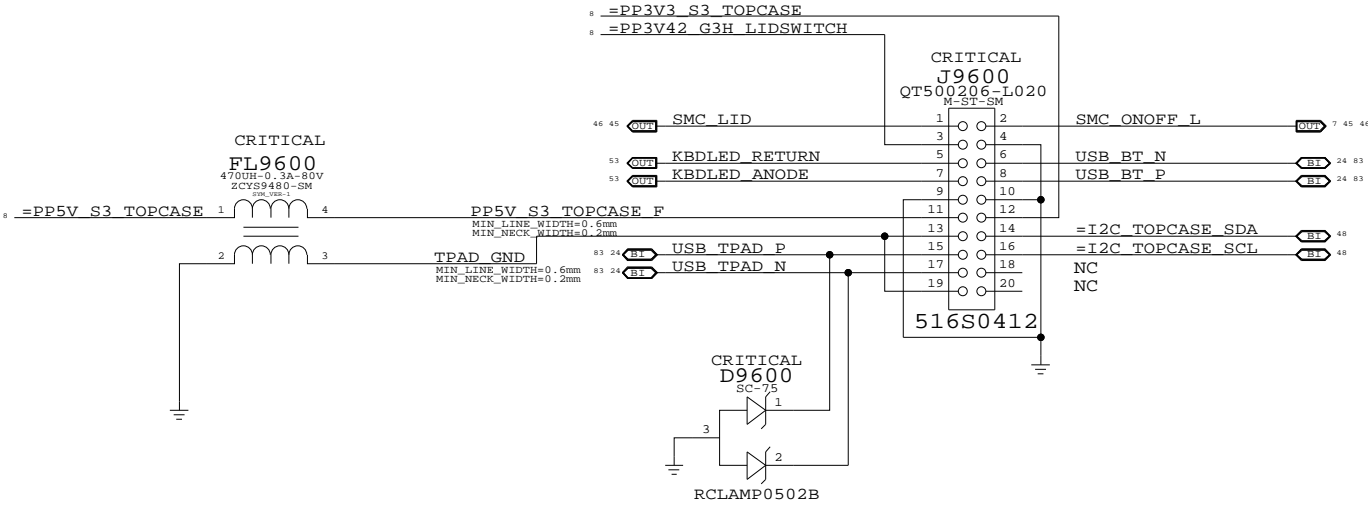
B

A

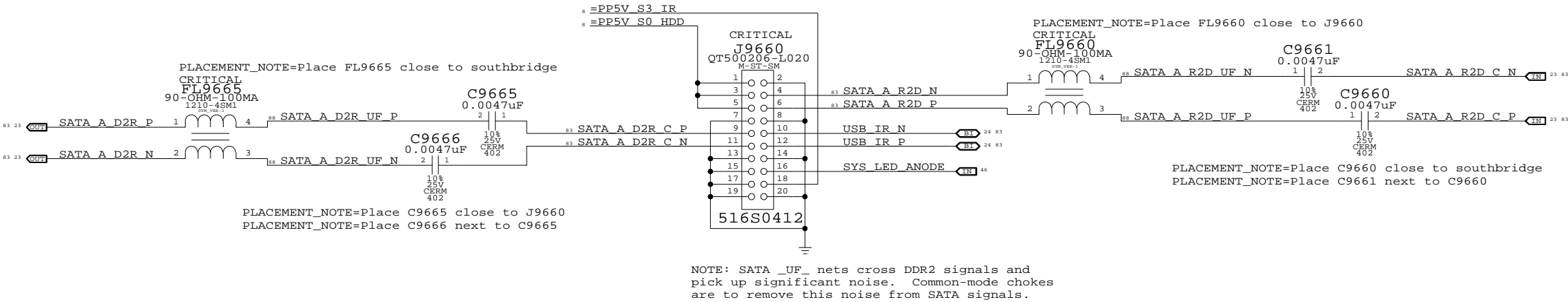
Left ALS Connector



Top-Case Connector



SATA HDD & IR & SIL Flex Connector



Project Specific Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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SIZE

D

DRAWING NUMBER

051-7413

REV.

15.0.0

SCALE

NONE

SHT

79

OF

89

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	= 3:1_SPACING	?
FSB_ADDR2ADDR	*	= 2:1_SPACING	?
FSB_ADSTB	*	= 3:1_SPACING	?
FSB_ADDR2ADSTB	*	= 3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_1TP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BNR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BPRI L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BREQ0 L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DBSY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DEFER L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DPWR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DRDY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HIT L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HITM L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB LOCK L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB RS L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB TRDY L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB CPURST L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTR0	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L P<0>	7 10 14
	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTR1	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L P<1>	7 10 14
	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTR2	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L P<2>	7 10 14
	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTR3	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L P<3>	7 10 14
	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTR0	FSB_55S	FSB_ADSTR	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTR1	FSB_55S	FSB_ADSTR	FSB ADSTB L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU IERR L	10
CPU_FERR_L	CPU_55S		CPU FERR L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2T01	CPU PROCHOT L	10 46 58
CPU_PWRGD	CPU_55S		CPU PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU INTR	10 23
CPU_FROM_SB	CPU_55S		CPU NMI	10 23
CPU_FROM_SB	CPU_55S		CPU A20M L	10 23
CPU_FROM_SB	CPU_55S		CPU DPSLP L	7 10 23
CPU_FROM_SB	CPU_55S		CPU IGNNL L	10 23
CPU_INIT_L	CPU_55S		CPU INIT L	10 23 47
CPU_FROM_SB	CPU_55S		CPU SMI L	10 23
CPU_FROM_SB	CPU_55S		CPU STPCLK L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2T01	PM THRMTRIP L	10 16 23 4
FSB_CPUSLP_L	CPU_55S		FSB CPUSLP L	7 10 14
PM DPRSLPVR	CPU_55S	CPU_2T01	PM DPRSLPVR	7 16 25 58
(See above)	CPU_55S	CPU_2T01	IMVP DPRSLPVR	58
CPU_BSEL0	CPU_55S	CPU_2T01	CPU BSEL<0>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<0>	13 16 3
CPU_BSEL1	CPU_55S	CPU_2T01	CPU BSEL<1>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2T01	CPU BSEL<2>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<2>	13 16 30
CPU DPRSTP_L	CPU_55S	CPU_2T01	CPU DPRSTP L	7 10 16 23
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP TRST L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP CLK P	13 30 85
	CLK_FSB_100D	CLK_FSB	XDP CLK N	13 30 85
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP CPURST L	13
	CPU_55S	CPU_2T01	CPU VID<6..0>	11 13
	CPU_55S	CPU_2T01	IMVP6_VID<6..0>	7 12 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 58
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	58
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	58

CPU/FSB Constraints

SYNC_MASTER=T9_NOME	SYNC_DATE=01/17/2007
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SCALE	SHT	OF
NONE	80	89

87654321

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.
CRT & TVDAC signal single-ended impedance varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG R2D P<15..0>	65
	PCIE_100D	PCIE	PEG R2D N<15..0>	65
	PCIE_100D	PCIE	PEG R2D_C P<15..0>	15 65
	PCIE_100D	PCIE	PEG R2D_C_N<15..0>	15 65
PEG_D2R	PCIE_100D	PCIE	PEG D2R P<15..0>	15 65
	PCIE_100D	PCIE	PEG D2R N<15..0>	15 65
	PCIE_100D	PCIE	PEG D2R_C P<15..0>	65
	PCIE_100D	PCIE	PEG D2R_C_N<15..0>	65
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0>	16 24
	DMI_100D	DMI	DMI N2S N<3..0>	16 24
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0>	16 24
	DMI_100D	DMI	DMI S2N N<3..0>	16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK P	15 22
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK N	15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0>	15 22
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0>	15 22
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3>	
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK P	15 22
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK N	15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA P<2..0>	15 22
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA N<2..0>	15 22
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA P<3>	
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA N<3>	
LVDS_IBG		LVDS	LVDS IBG	15 22
CRT_TVO_IREF		CRT	CRT TVO IREF	
CRT_RED	CRT_50S	CRT	CRT RED	
CRT_GREEN	CRT_50S	CRT	CRT GREEN	
CRT_BLUE	CRT_50S	CRT	CRT BLUE	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC R	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC R	
TV_A_DAC	CRT_50S	TVDAC	TV A DAC	
TV_B_DAC	CRT_50S	TVDAC	TV B DAC	
TV_C_DAC	CRT_50S	TVDAC	TV C DAC	

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7413	15.0.0
SCALE	SHT	OF
NONE	81	89

87654321

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20THER
MEM_CTRL	*	*	MEM_20THER
MEM_CMD	*	*	MEM_20THER
MEM_DATA	*	*	MEM_20THER
MEM_DQS	*	*	MEM_20THER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM CLK P<2..0>	16	31
	MEM_70D	MEM_CLK	MEM CLK N<2..0>	16	31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16	31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM CS L<31..0>	16	31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM ODT<1..0>	16	31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A A<14..0>	16	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A BS<2..0>	17	31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A RAS L	17	31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A CAS L	17	31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A WE L	17	31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>	17	31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>	17	31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>	17	31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>	17	31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>	17	31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>	17	31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>	17	31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>	17	31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM A DM<0>	17	31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM A DM<1>	17	31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM A DM<2>	17	31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM A DM<3>	17	31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM A DM<4>	17	31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM A DM<5>	17	31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM A DM<6>	17	31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM A DM<7>	17	31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	17	31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	17	31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	17	31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	17	31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	17	31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	17	31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	17	31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	17	31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	17	31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	17	31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	17	31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	17	31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	17	31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	17	31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	17	31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	17	31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM CLK P<5..3>	16	32
MEM_B_CLK	MEM_70D	MEM_CLK	MEM CLK N<5..3>	16	32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16	32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM CS L<3..2>	16	32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM ODT<3..2>	16	32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B A<14..0>	16	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B BS<2..0>	17	32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B RAS L	17	32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B CAS L	17	32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B WE L	17	32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>	17	32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>	17	32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>	17	32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>	17	32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>	17	32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>	17	32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>	17	32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>	17	32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM B DM<0>	17	32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM B DM<1>	17	32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM B DM<2>	17	32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM B DM<3>	17	32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM B DM<4>	17	32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM B DM<5>	17	32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM B DM<6>	17	32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM B DM<7>	17	32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	17	32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	17	32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	17	32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	17	32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	17	32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	17	32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	17	32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	17	32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	17	32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	17	32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	17	32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	17	32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	17	32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	17	32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	17	32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	17	32

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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APPLE INC.

SIZE
D

NUMBER
051-7413

REV.
15.0.0

SCALE	
NONE	

SHT	8
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OF 89

87654321

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
<input type="checkbox"/> FW_D_CTL	FW_55S	FW	FW LINK<7..0>
<input type="checkbox"/> FW_D_CTL	FW_55S	FW	FW CTL<1..0>
<input type="checkbox"/> FW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK LCLK
<input type="checkbox"/> FW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY LCLK3839
<input type="checkbox"/> FW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK PCLK3839
<input type="checkbox"/> FW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY PCLK
<input type="checkbox"/> FW_LKON	FW_55S	FW	FW LKON
<input type="checkbox"/> FW_LKON	FW_55S	FW	FW LKON R
<input type="checkbox"/> FW_LPS	FW_55S	FW	FW LPS3839
<input type="checkbox"/> FW_LREQ	FW_55S	FW	FW LREQ3839
<input type="checkbox"/> FW_PINT	FW_55S	FW	FW PINT3839
<input type="checkbox"/> FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M FW XI_R
<input type="checkbox"/> FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M FW XI
<input type="checkbox"/> FW_0_TPA	FW_110D	FW_TP	FW 0 TPA_P3941
<input type="checkbox"/> FW_0_TPA	FW_110D	FW_TP	FW 0 TPA_N3941
<input type="checkbox"/> FW_0_TPB	FW_110D	FW_TP	FW 0 TPB_P3941
<input type="checkbox"/> FW_0_TPB	FW_110D	FW_TP	FW 0 TPB_N3941
<input type="checkbox"/> FW_1_TPA	FW_110D	FW_TP	FW 1 TPA_P3941
<input type="checkbox"/> FW_1_TPA	FW_110D	FW_TP	FW 1 TPA_N3941
<input type="checkbox"/> FW_1_TPB	FW_110D	FW_TP	FW 1 TPB_P3941
<input type="checkbox"/> FW_1_TPB	FW_110D	FW_TP	FW 1 TPB_N3941
Port 2 Not Used			

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FireWire Constraints

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SIZE	D	DRAWING NUMBER	051-7413	REV.	15.0.0
SCALE	NONE	SHT	86	OF	89

87654321

8		7		6		5		4		3		2		1	
M75 Board-Specific Spacing & Physical Constraints															
BOARD LAYERS								BOARD AREAS				BOARD UNITS (MIL or MM)		ALLEGRO VERSION	
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM								NO_TYPE, BGA				MM		15.5.1	
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
DEFAULT		*	Y	=55_OHM_SE		=55_OHM_SE		30 MM		0 MM		0 MM			
STANDARD		*	Y	=DEFAULT		=DEFAULT		12.7 MM		=DEFAULT		=DEFAULT			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
55_OHM_SE		TOP, BOTTOM	Y	0.100 MM		0.100 MM									
55_OHM_SE		ISL2, ISL11	Y	0.250 MM		0.076 MM									
55_OHM_SE		*	Y	0.076 MM		0.076 MM		=STANDARD		=STANDARD		=STANDARD			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
50_OHM_SE		TOP, BOTTOM	Y	0.125 MM		0.125 MM									
50_OHM_SE		*	Y	0.090 MM		0.090 MM		=STANDARD		=STANDARD		=STANDARD			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
46_OHM_SE		TOP, BOTTOM	Y	0.126 MM		0.126 MM									
46_OHM_SE		*	Y	0.100 MM		0.100 MM		=STANDARD		=STANDARD		=STANDARD			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
45_OHM_SE		TOP, BOTTOM	Y	0.150 MM		0.150 MM									
45_OHM_SE		*	Y	0.105 MM		0.105 MM		=STANDARD		=STANDARD		=STANDARD			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
40_OHM_SE		TOP, BOTTOM	Y	0.185 MM		0.185 MM									
40_OHM_SE		*	Y	0.131 MM		0.131 MM		=STANDARD		=STANDARD		=STANDARD			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
27P4_OHM_SE		TOP, BOTTOM	Y	0.335 MM		0.335 MM									
27P4_OHM_SE		*	Y	0.240 MM		0.240 MM		=STANDARD		=STANDARD		=STANDARD			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
70_OHM_DIFF		*	N	=STANDARD		=STANDARD		=STANDARD		=STANDARD		=STANDARD			
70_OHM_DIFF		ISL3, ISL4	Y	0.149 MM		0.149 MM				0.125 MM		0.125 MM			
70_OHM_DIFF		ISL9, ISL10	Y	0.149 MM		0.149 MM				0.125 MM		0.125 MM			
70_OHM_DIFF		ISL2, ISL11	Y	0.185 MM		0.185 MM				0.125 MM		0.125 MM			
70_OHM_DIFF		TOP, BOTTOM	Y	0.185 MM		0.185 MM				0.125 MM		0.125 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
80_OHM_DIFF		*	N	=STANDARD		=STANDARD		=STANDARD		=STANDARD		=STANDARD			
80_OHM_DIFF		ISL3, ISL4	Y	0.115 MM		0.115 MM				0.125 MM		0.125 MM			
80_OHM_DIFF		ISL9, ISL10	Y	0.115 MM		0.115 MM				0.125 MM		0.125 MM			
80_OHM_DIFF		ISL2, ISL11	Y	0.140 MM		0.140 MM				0.125 MM		0.125 MM			
80_OHM_DIFF		TOP, BOTTOM	Y	0.140 MM		0.140 MM				0.125 MM		0.125 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
85_OHM_DIFF		*	N	=STANDARD		=STANDARD		=STANDARD		=STANDARD		=STANDARD			
85_OHM_DIFF		ISL3, ISL4	Y	0.101 MM		0.101 MM				0.125 MM		0.125 MM			
85_OHM_DIFF		ISL9, ISL10	Y	0.101 MM		0.101 MM				0.125 MM		0.125 MM			
85_OHM_DIFF		ISL2, ISL11	Y	0.125 MM		0.125 MM				0.125 MM		0.125 MM			
85_OHM_DIFF		TOP, BOTTOM	Y	0.125 MM		0.125 MM				0.125 MM		0.125 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
90_OHM_DIFF		*	N	=STANDARD		=STANDARD		=STANDARD		=STANDARD		=STANDARD			
90_OHM_DIFF		ISL3, ISL4	Y	0.102 MM		0.102 MM				0.220 MM		0.220 MM			
90_OHM_DIFF		ISL9, ISL10	Y	0.102 MM		0.102 MM				0.220 MM		0.220 MM			
90_OHM_DIFF		ISL2, ISL11	Y	0.130 MM		0.130 MM				0.220 MM		0.220 MM			
90_OHM_DIFF		TOP, BOTTOM	Y	0.130 MM		0.130 MM				0.220 MM		0.220 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
100_OHM_DIFF		*	N	=STANDARD		=STANDARD		=STANDARD		=STANDARD		=STANDARD			
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM		0.080 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		ISL2, ISL11	Y	0.099 MM		0.099 MM				0.200 MM		0.200 MM			
100_OHM_DIFF		TOP, BOTTOM	Y	0.099 MM		0.099 MM				0.200 MM		0.200 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
110_OHM_DIFF		*	N	=STANDARD		=STANDARD		=STANDARD		=STANDARD		=STANDARD			
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM		0.077 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		ISL2, ISL11	Y	0.089 MM		0.089 MM				0.330 MM		0.330 MM			
110_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM		0.089 MM				0.330 MM		0.330 MM			
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH		MINIMUM NECK WIDTH		MAXIMUM NECK LENGTH		DIFFPAIR PRIMARY GAP		DIFFPAIR NECK GAP			
100_DIFF_BGA		*	=100_OHM_DIFF	=100_OHM_DIFF		=100_OHM_DIFF		=100_OHM_DIFF		=100_OHM_DIFF		=100_OHM_DIFF			
100_DIFF_BGA		ISL3, ISL4	Y	0.075 MM		0.075 MM				0.125 MM		0.125 MM			
100_DIFF_BGA		ISL9, ISL10	Y	0.075 MM		0.075 MM				0.125 MM		0.125 MM			
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.															
PCB Rule Definitions															
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)															
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SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DEFAULT	*	0.1 MM	?	*	*	BGA	BGA_P1MM
STANDARD	*	=DEFAULT	?	MEM_CLK	*	BGA	BGA_P2MM
BGA_P1MM	*	=DEFAULT	?	CLK_FSB	*	BGA	BGA_P2MM
BGA_P2MM	*	=DEFAULT	?	CLK_PCIE	*	BGA	BGA_P2MM
BGA_P3MM	*	=DEFAULT	?	CLK_MED	*	BGA	BGA_P2MM
				CLK_SLOW	*	BGA	BGA_P2MM
				FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

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